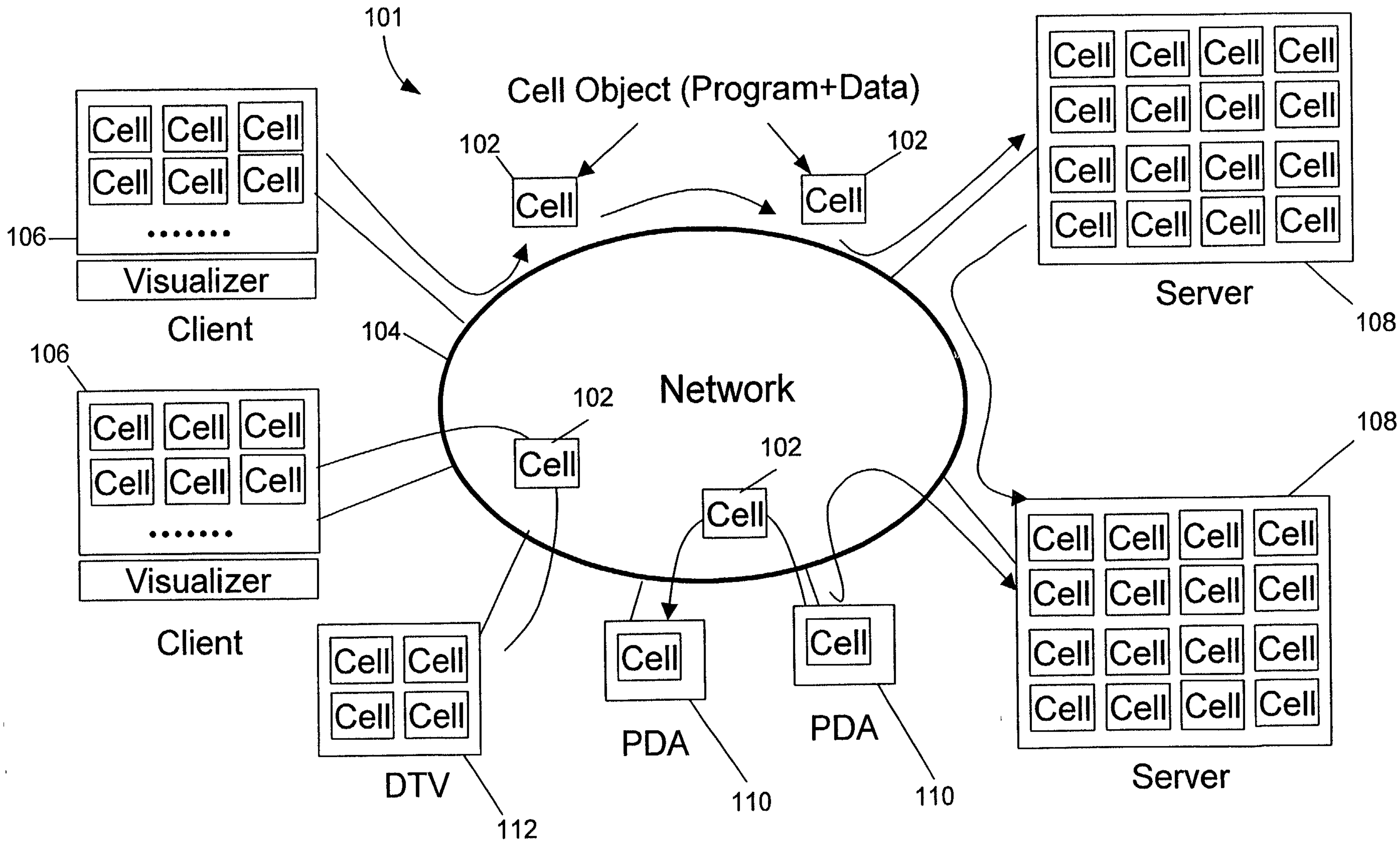
101
Cell Object (Program+Data)
102
Cell
102
Cell
106
Cell
Visualizer
Client
106
Cell
Visualizer
Client
104
Network
102
Cell
102
Cell
DTV
112
PDA
110
PDA
110
Server
108
Server
108

FIG. 1

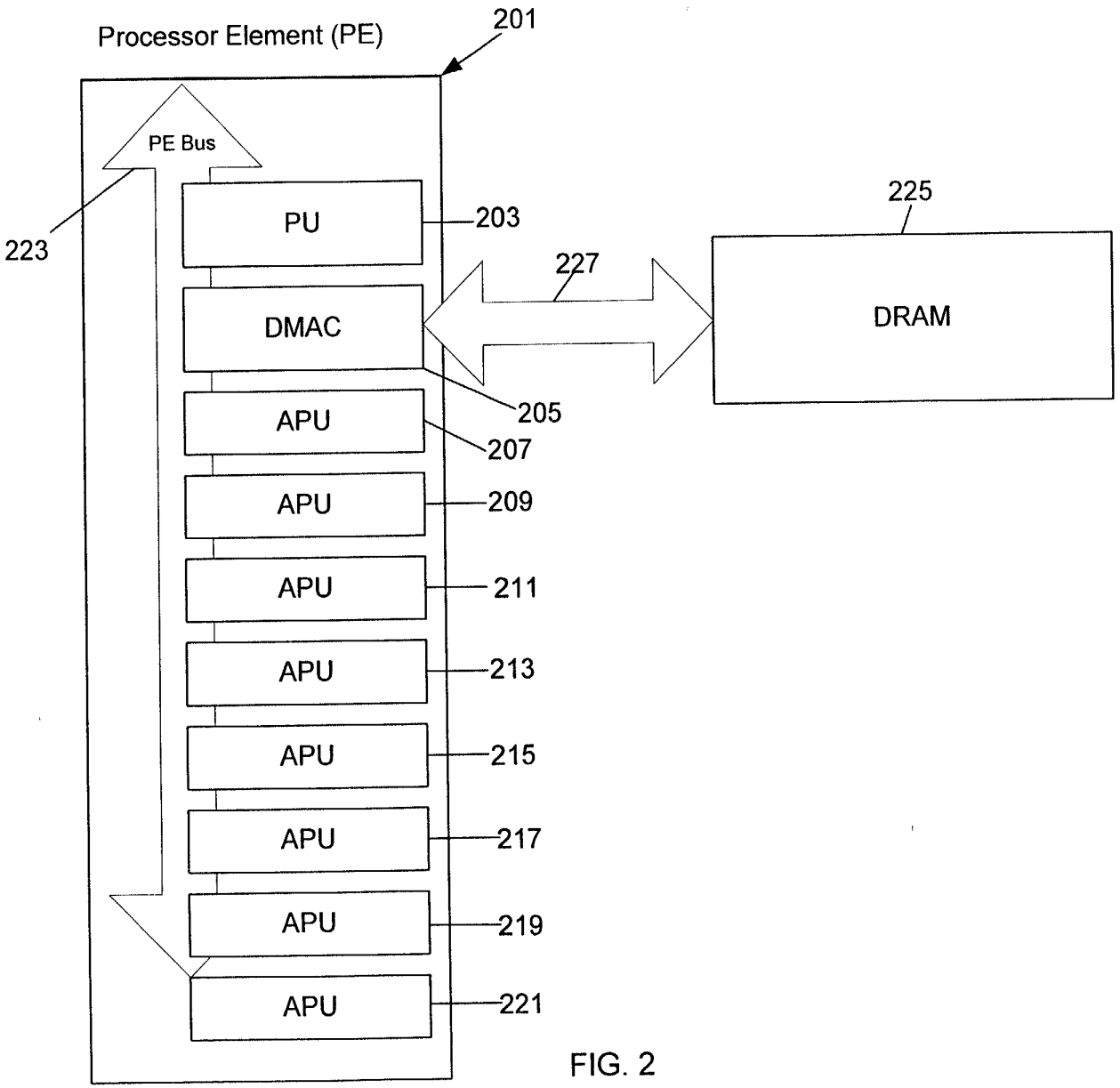

FIG. 2

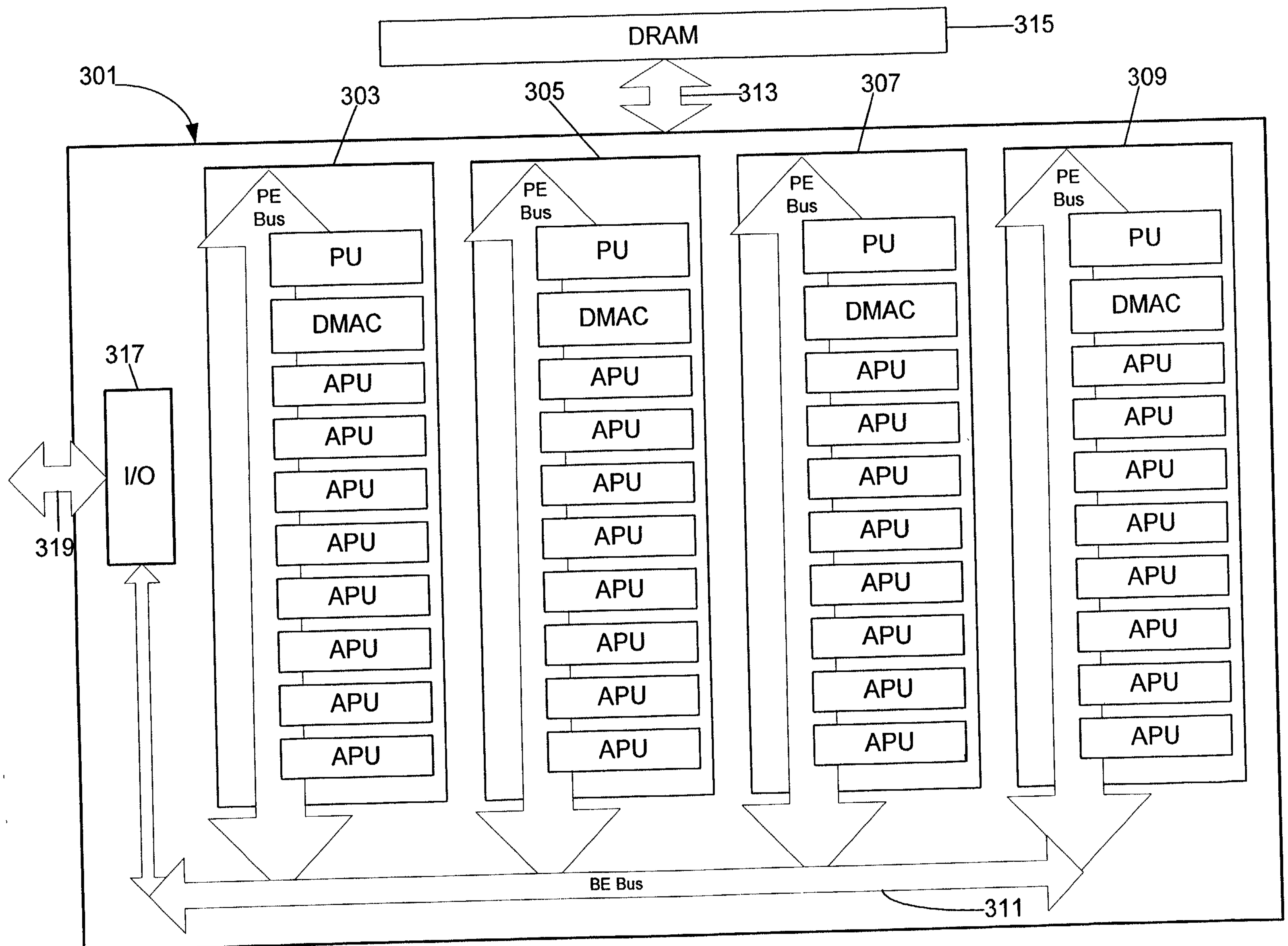
DRAM
315
301
303
305
313
307
309
PE
Bus
PU
DMAC
APU
APU
APU
APU
APU
APU
APU
APU
PE
Bus
PU
DMAC
APU
APU
APU
APU
APU
APU
APU
APU
PE
Bus
PU
DMAC
APU
APU
APU
APU
APU
APU
APU
APU
PE
Bus
PU
DMAC
APU
APU
APU
APU
APU
APU
APU
APU
317
I/O
319
BE Bus
311

FIG. 3

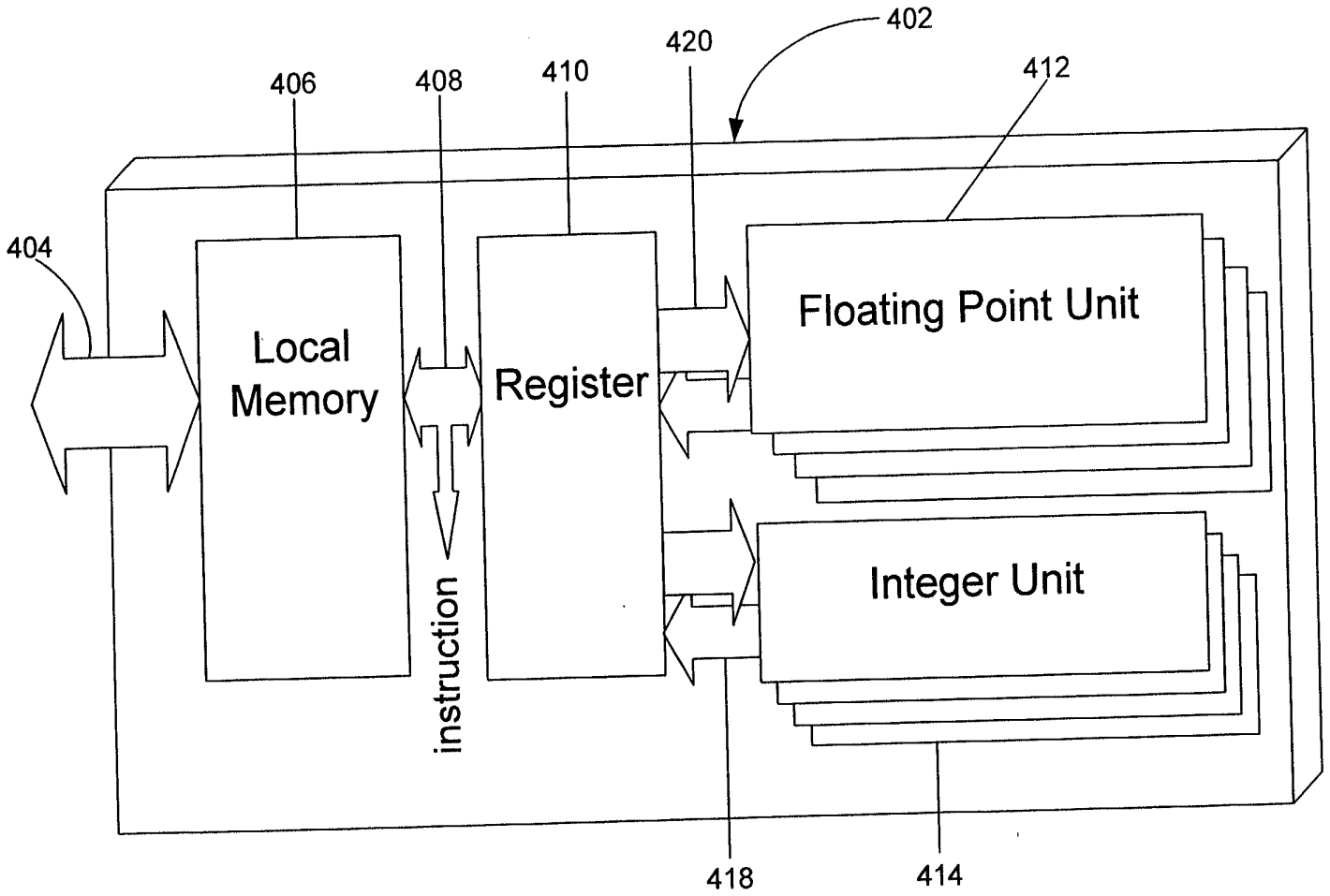
402
420
406
408
410
412
404
Local Memory
Register
Floating Point Unit
Integer Unit
instruction
418
414

FIG. 4

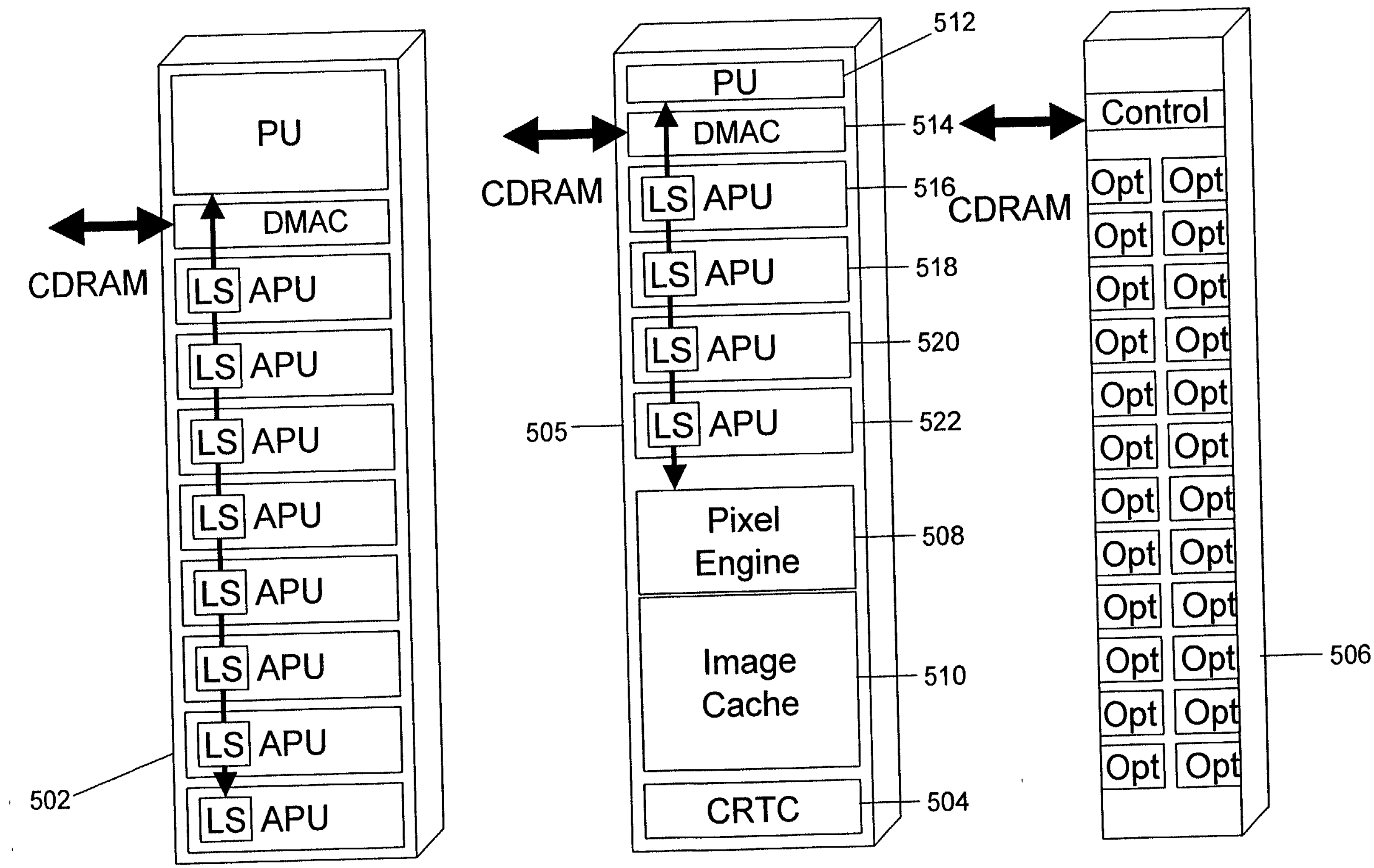
PU
DMAC
CDRAM
LS
APU
502
512
514
516
518
520
522
505
Pixel
Engine
Image
Cache
CRTC
508
510
504
Control
Opt
506

FIG. 5

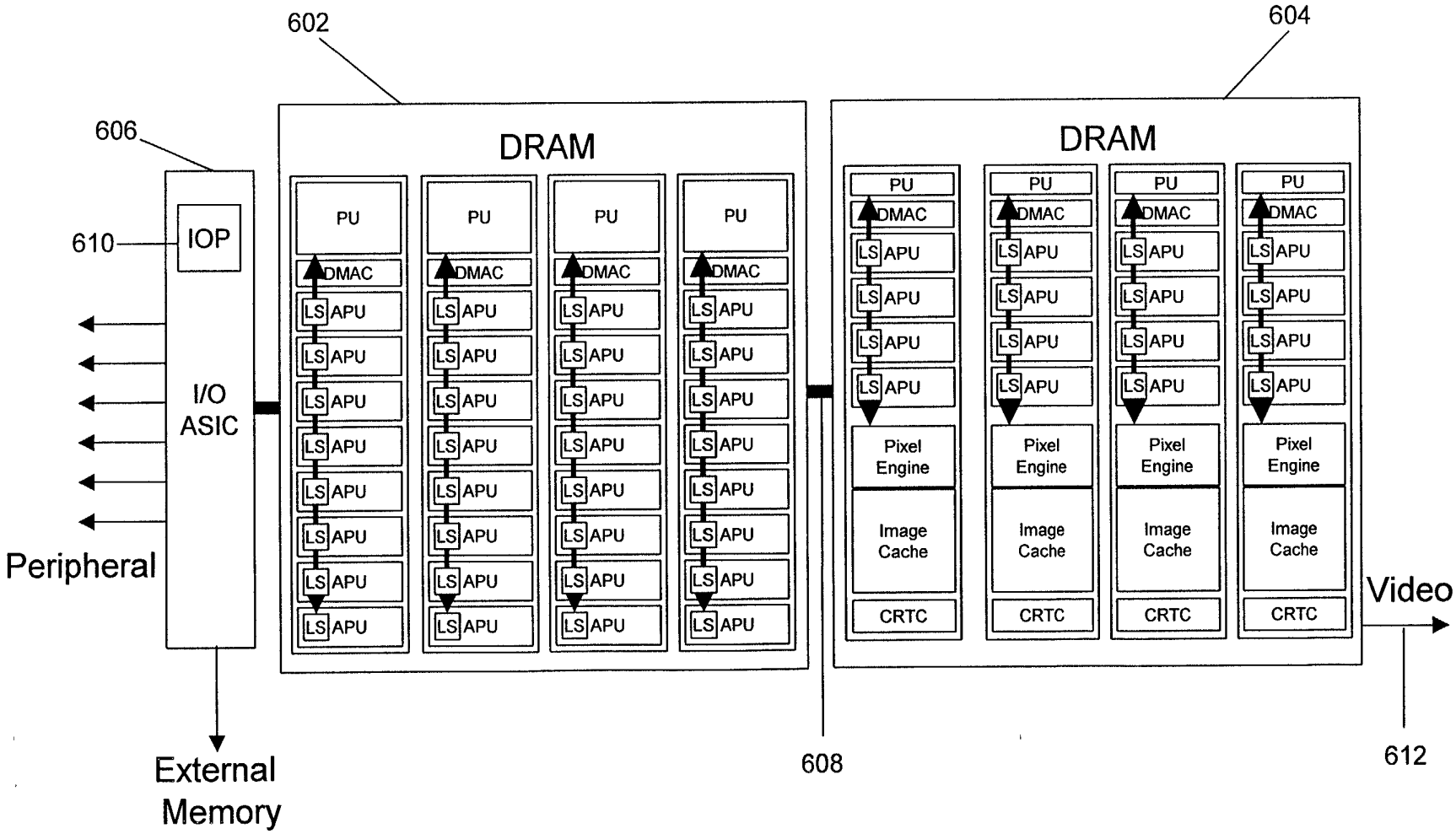
602
604
606
610
DRAM
DRAM
IOP
I/O
ASIC
PU
DMAC
LS
APU
Pixel
Engine
Image
Cache
CRTC
Peripheral
External
Memory
608
Video
612

FIG. 6

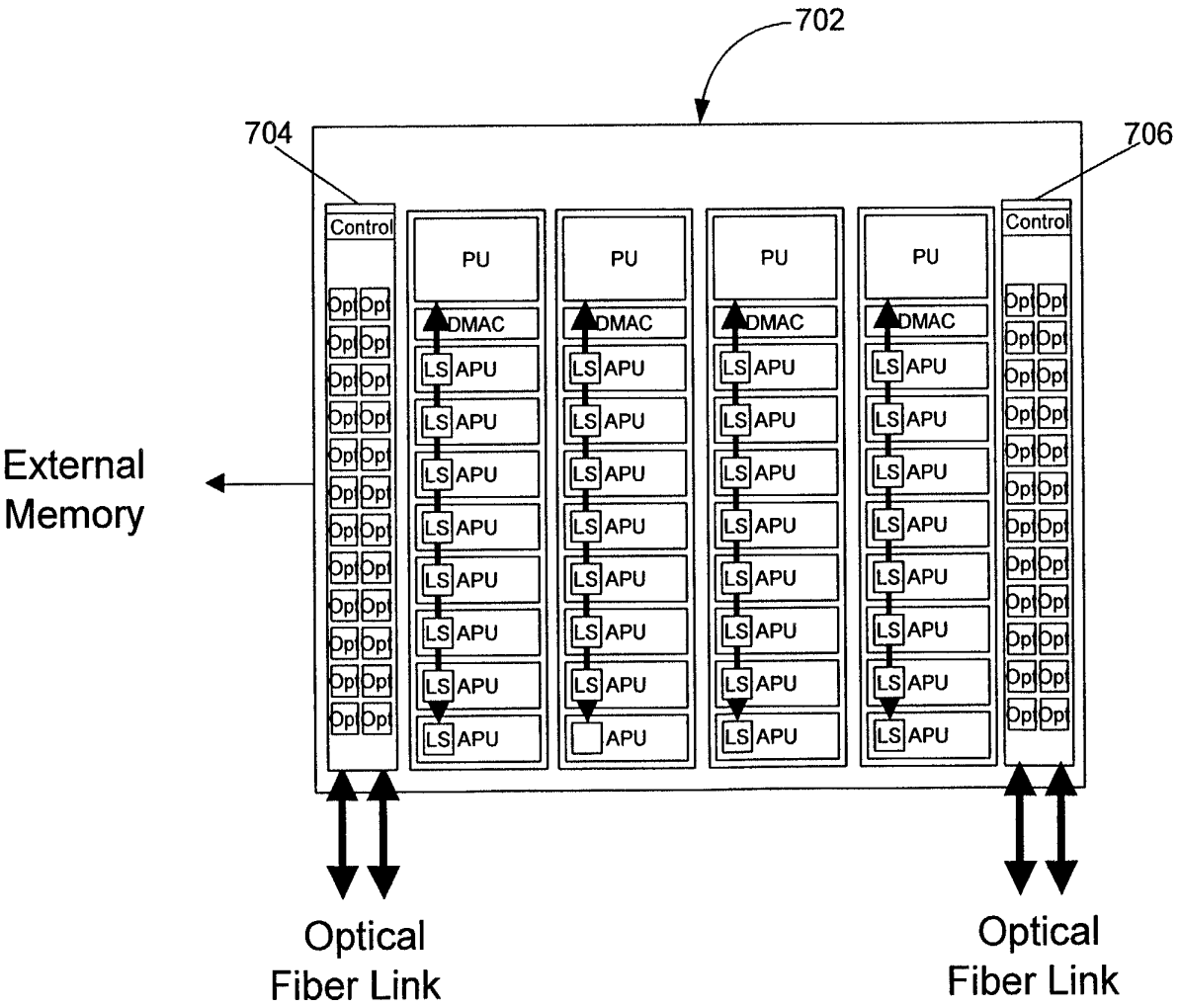

FIG. 7

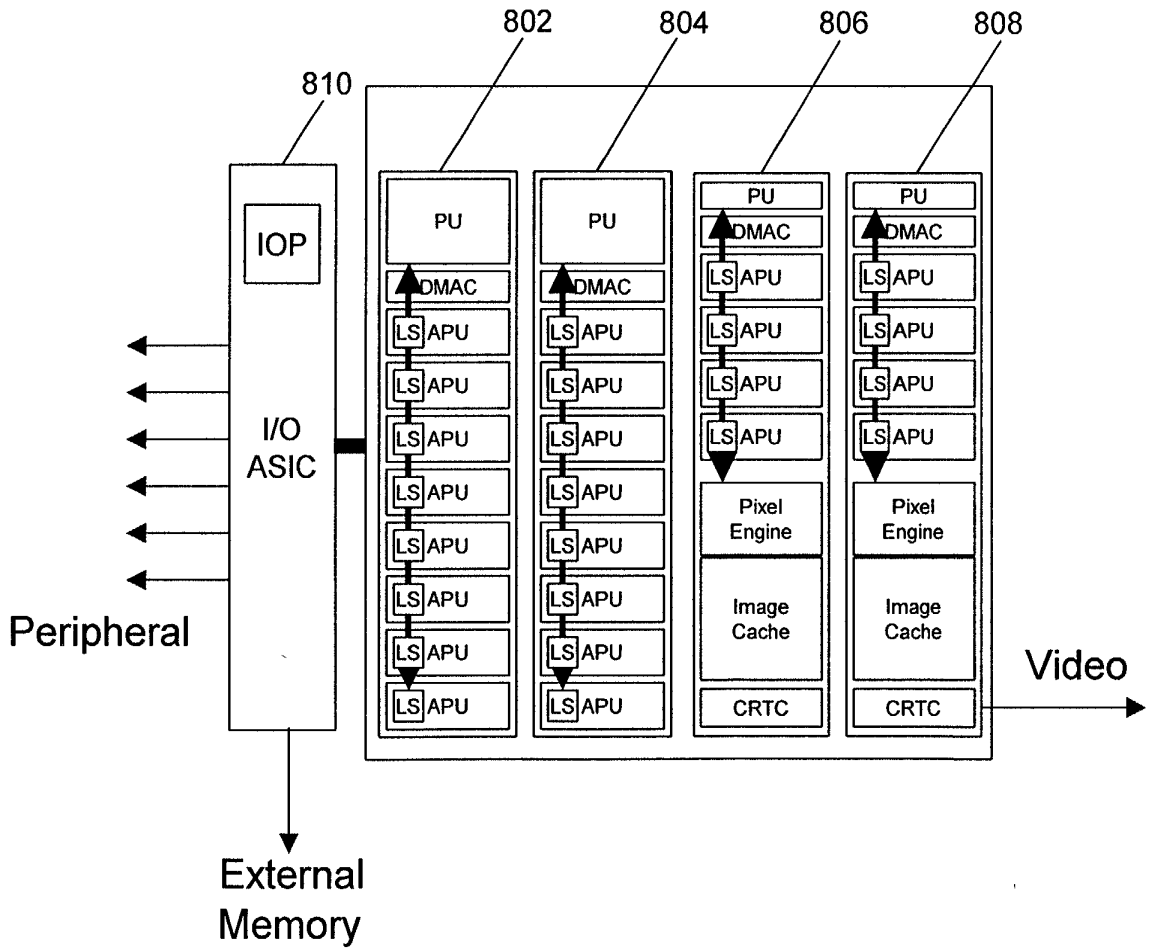

FIG. 8

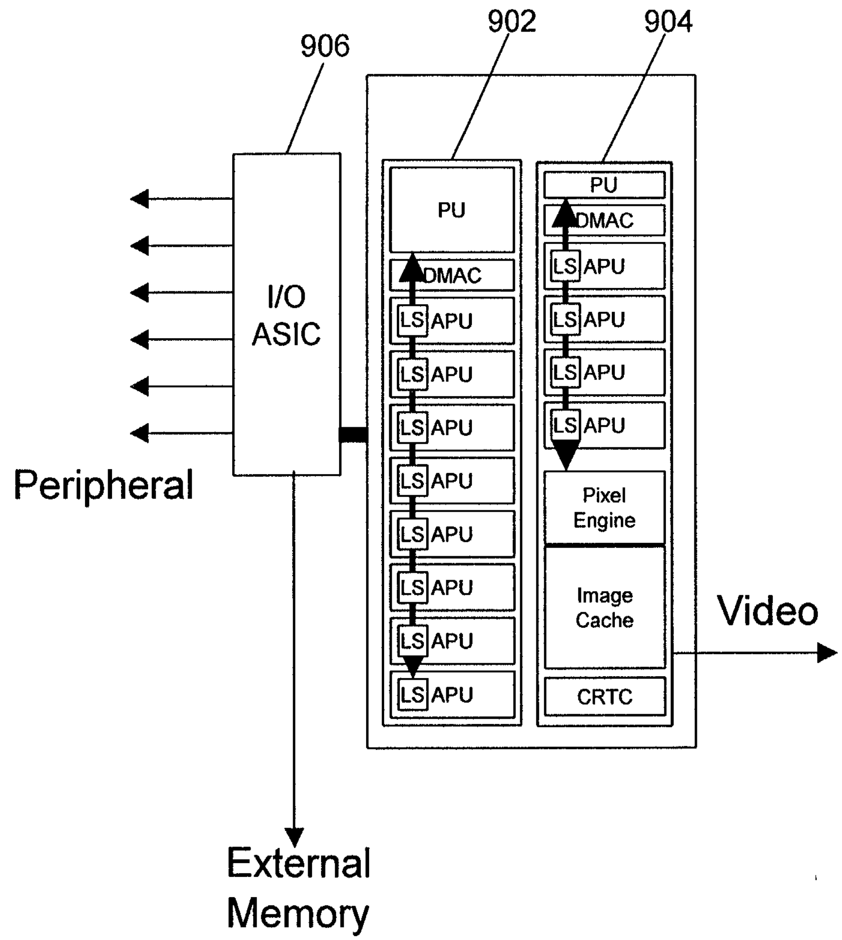
906
902
904
I/O
ASIC
Peripheral
External
Memory
PU
DMAC
LS
APU
Pixel
Engine
Image
Cache
CRTC
Video

FIG. 9

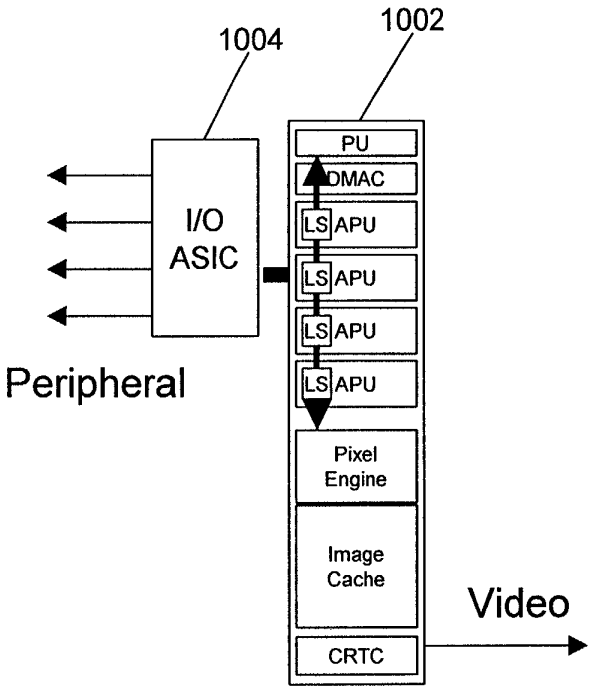

FIG. 10

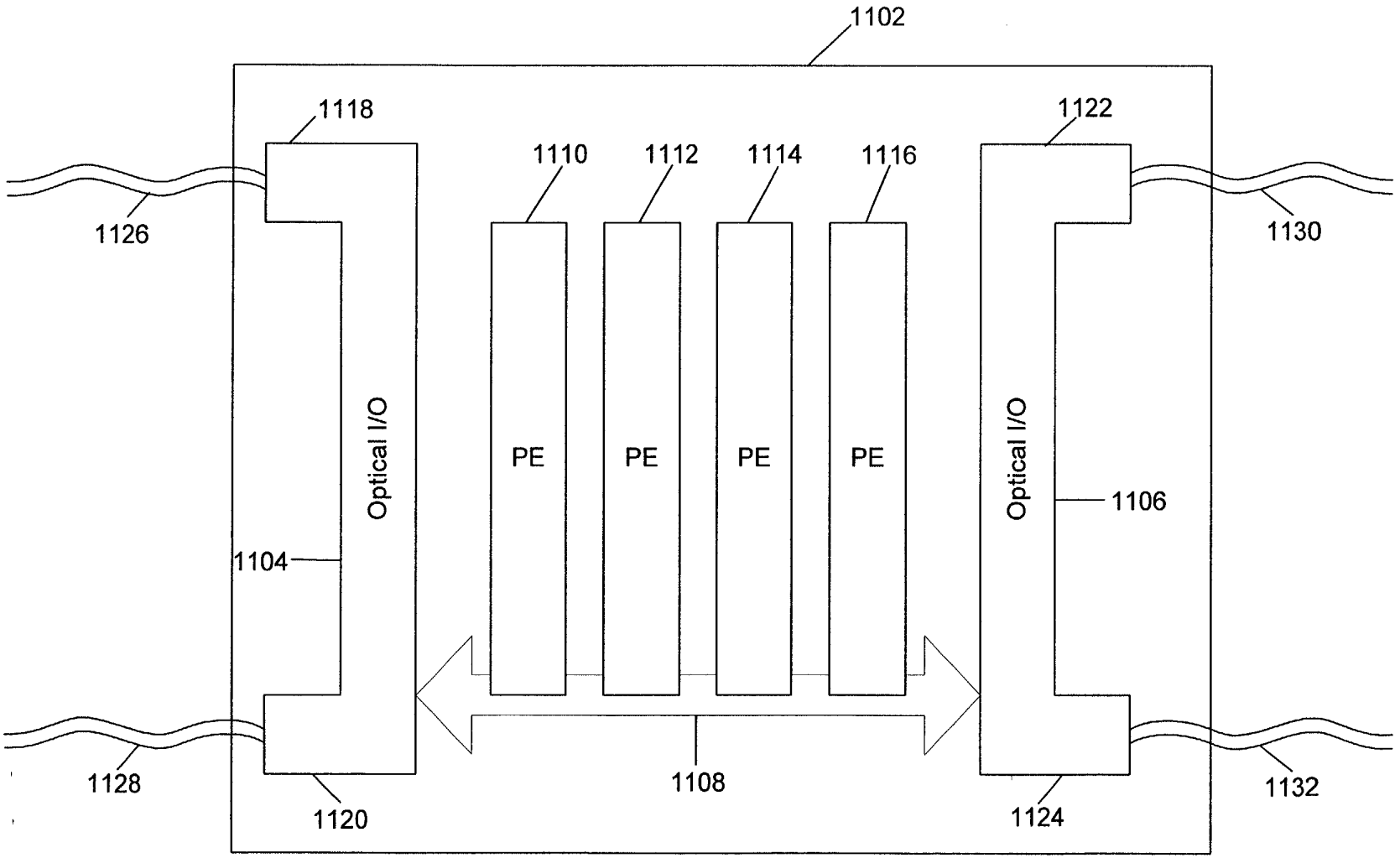

FIG. 11A

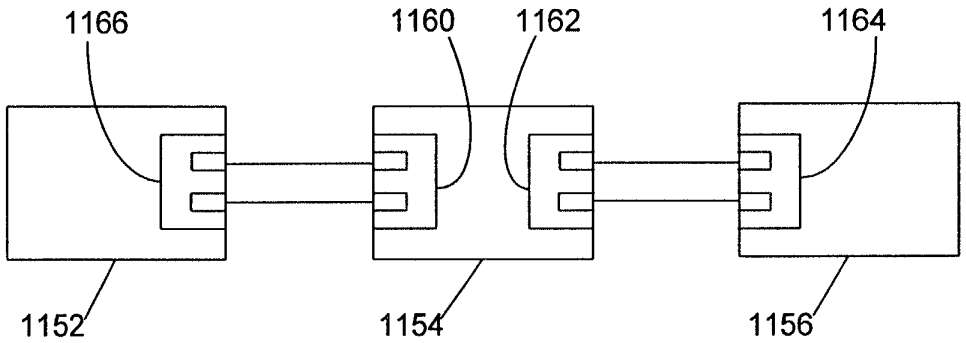

FIG. 11B

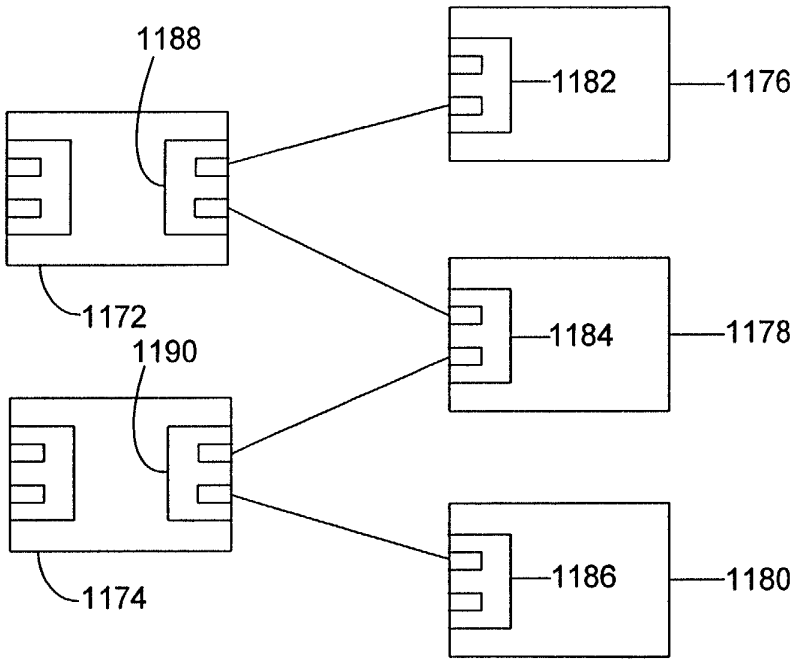

FIG. 11C

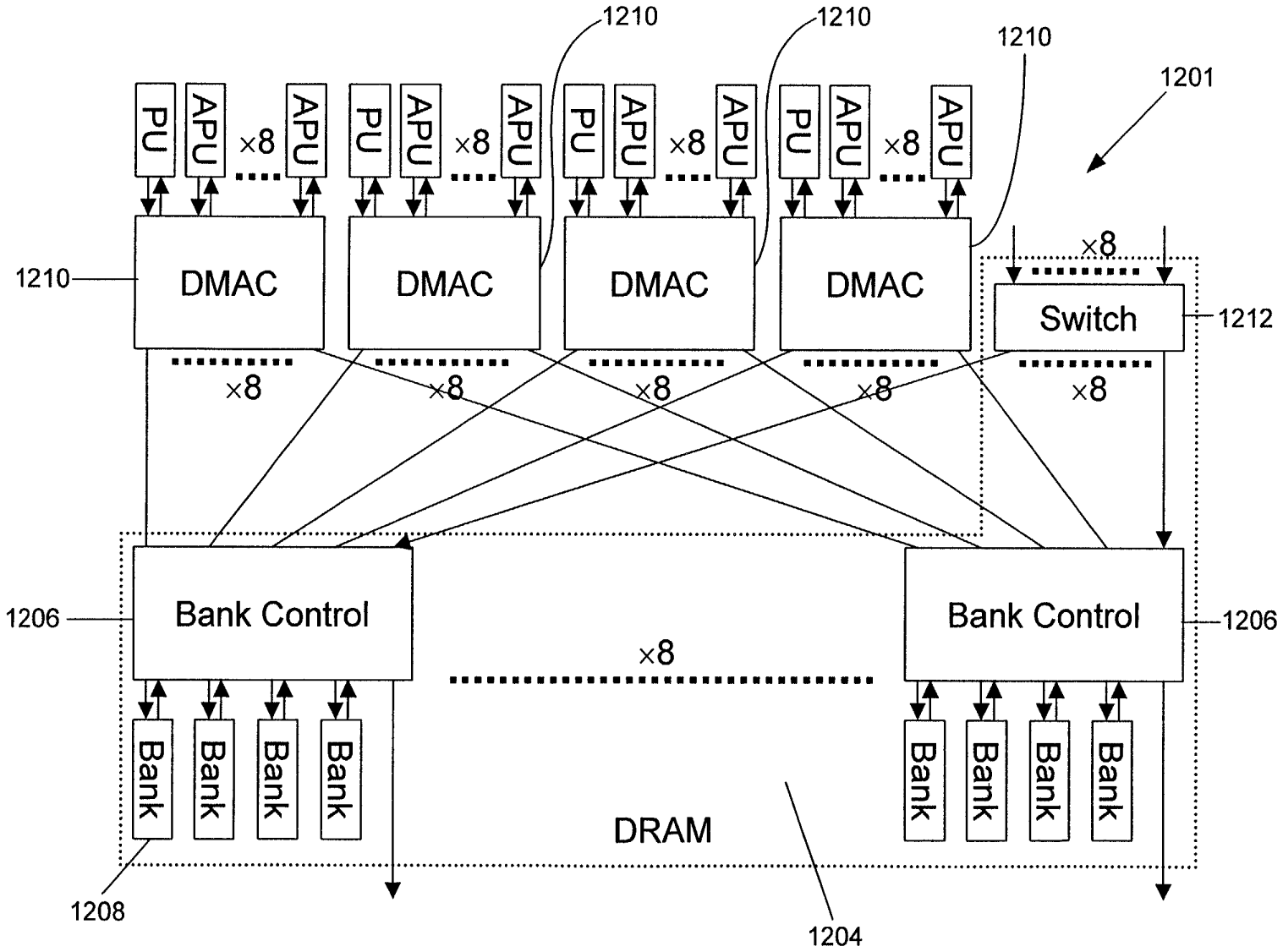
1210
1210
1210
1201
PU
APU
×8
APU
DMAC
DMAC
DMAC
DMAC
1210
×8
Switch
1212
×8
×8
×8
×8
×8
1206
Bank Control
Bank Control
1206
×8
Bank
Bank
Bank
Bank
Bank
Bank
Bank
Bank
DRAM
1208
1204

FIG. 12A

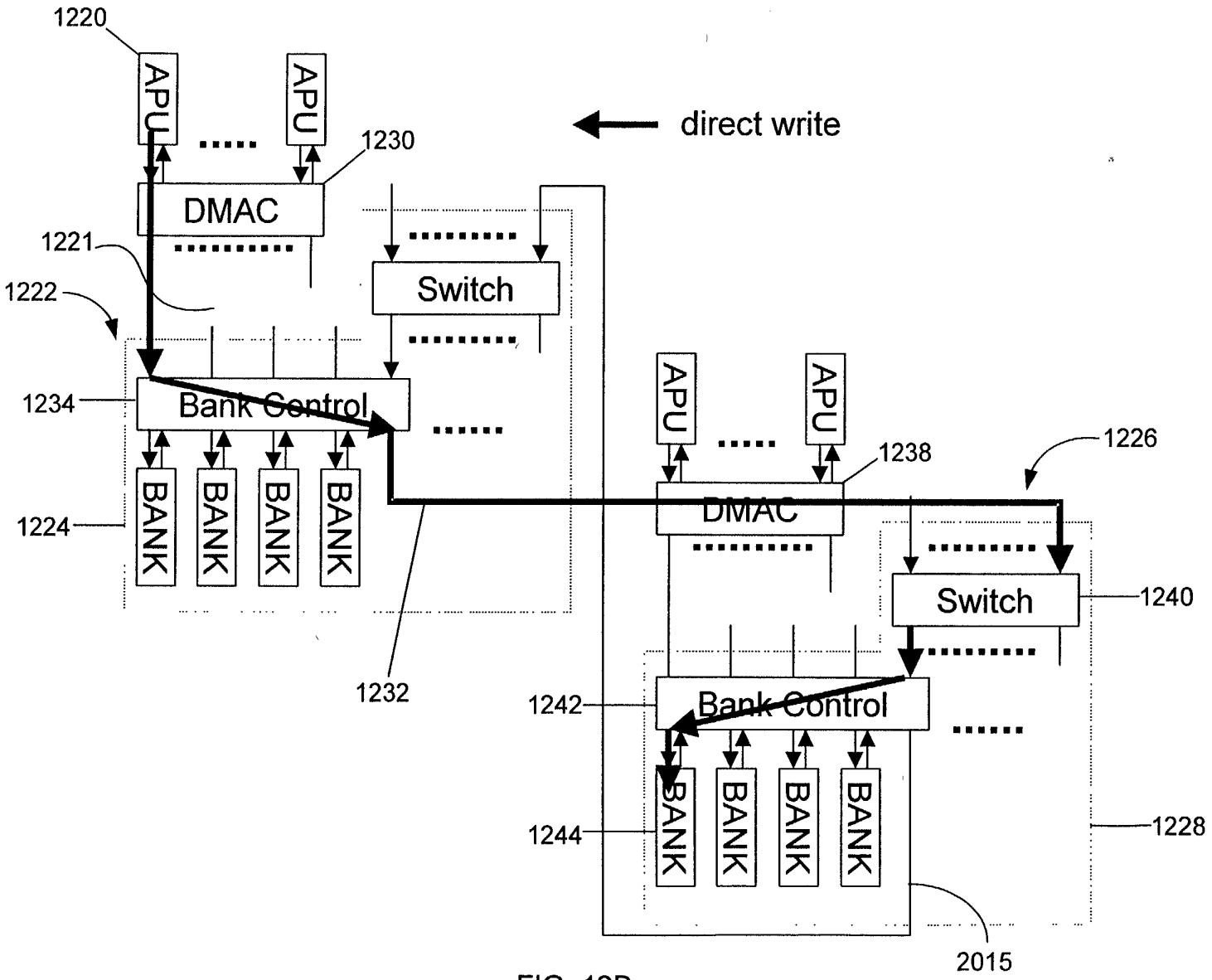
1220
APU
APU
direct write
1230
DMAC
1221
1222
Switch
1234
Bank Control
APU
APU
1238
1226
1224
BANK
BANK
BANK
BANK
DMAC
Switch
1240
1232
1242
Bank Control
1244
BANK
BANK
BANK
BANK
1228
2015

FIG. 12B

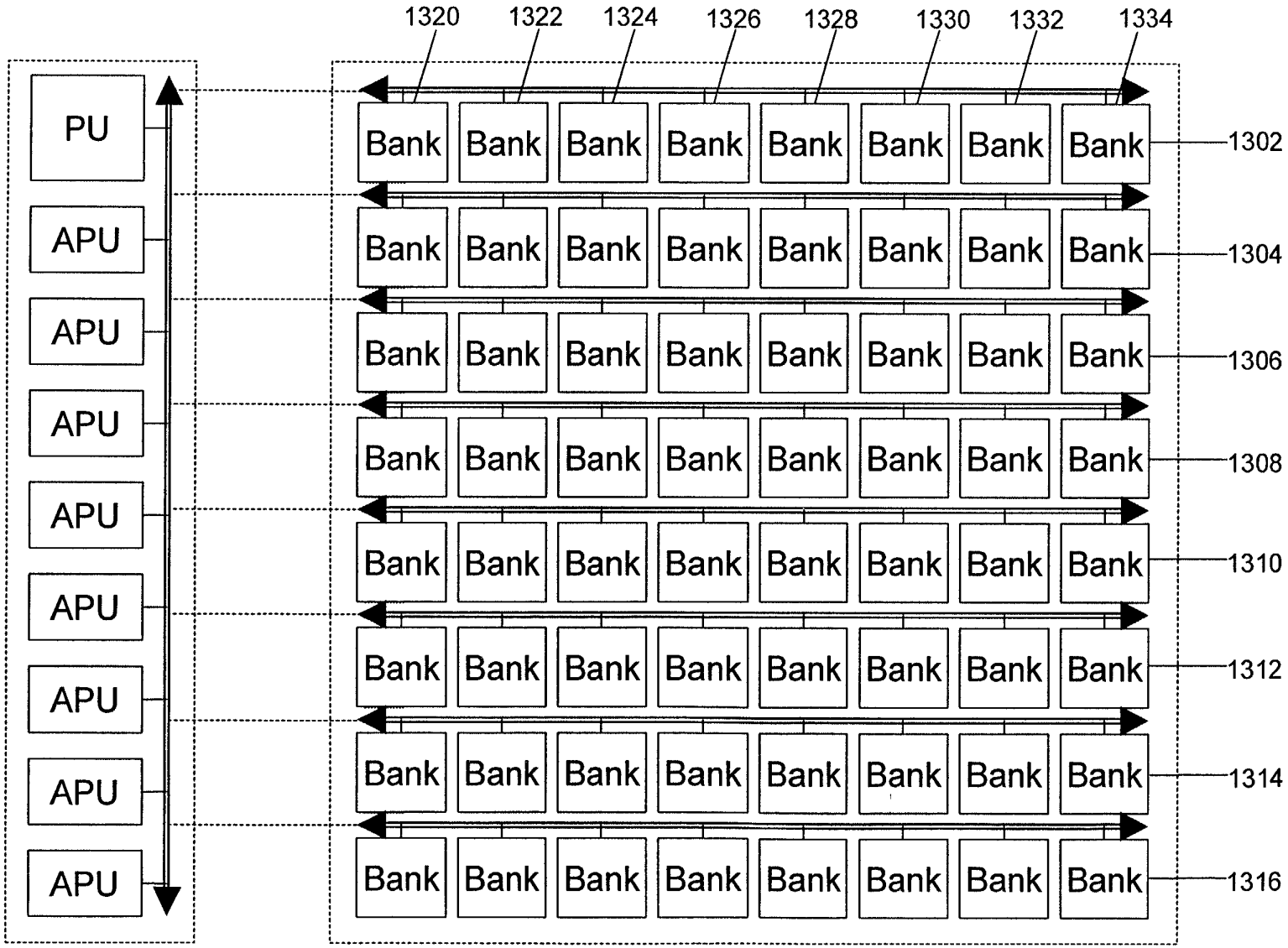
1320
1322
1324
1326
1328
1330
1332
1334
PU
APU
APU
APU
APU
APU
APU
APU
APU
Bank
1302
1304
1306
1308
1310
1312
1314
1316
DRAM

FIG. 13

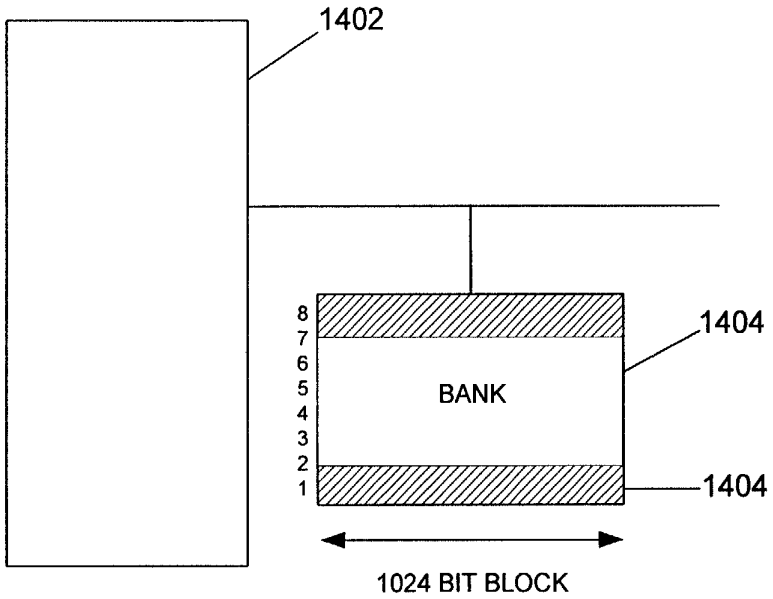

FIG. 14A

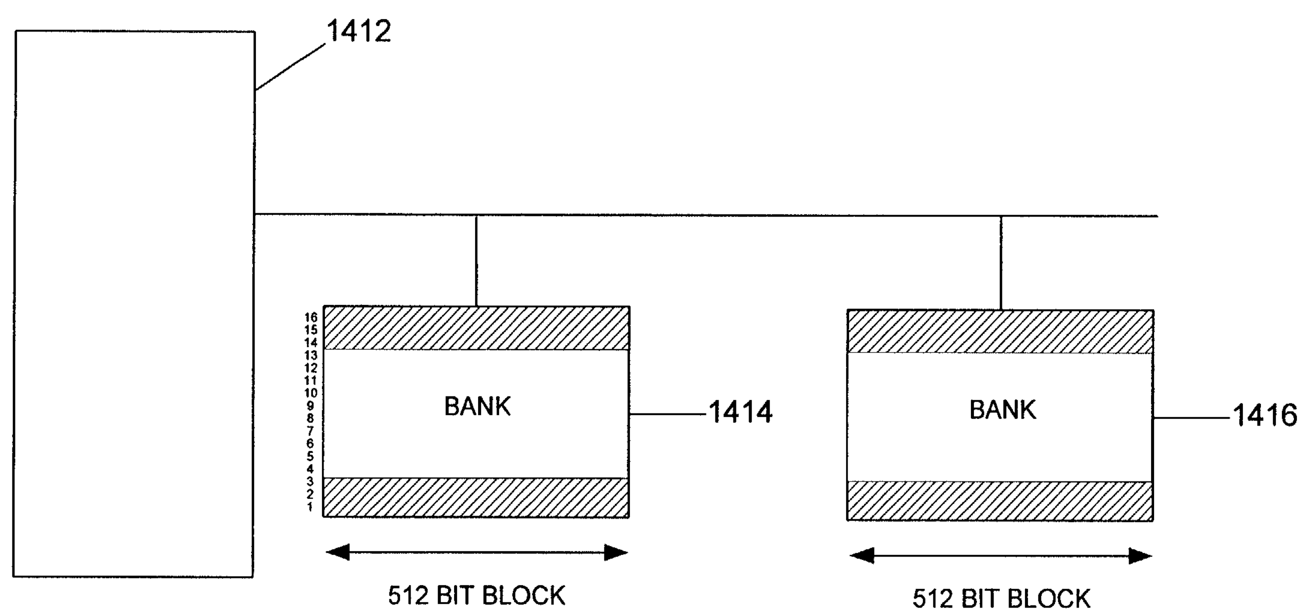
1412
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
BANK
1414
512 BIT BLOCK
BANK
1416
512 BIT BLOCK

FIG. 14B

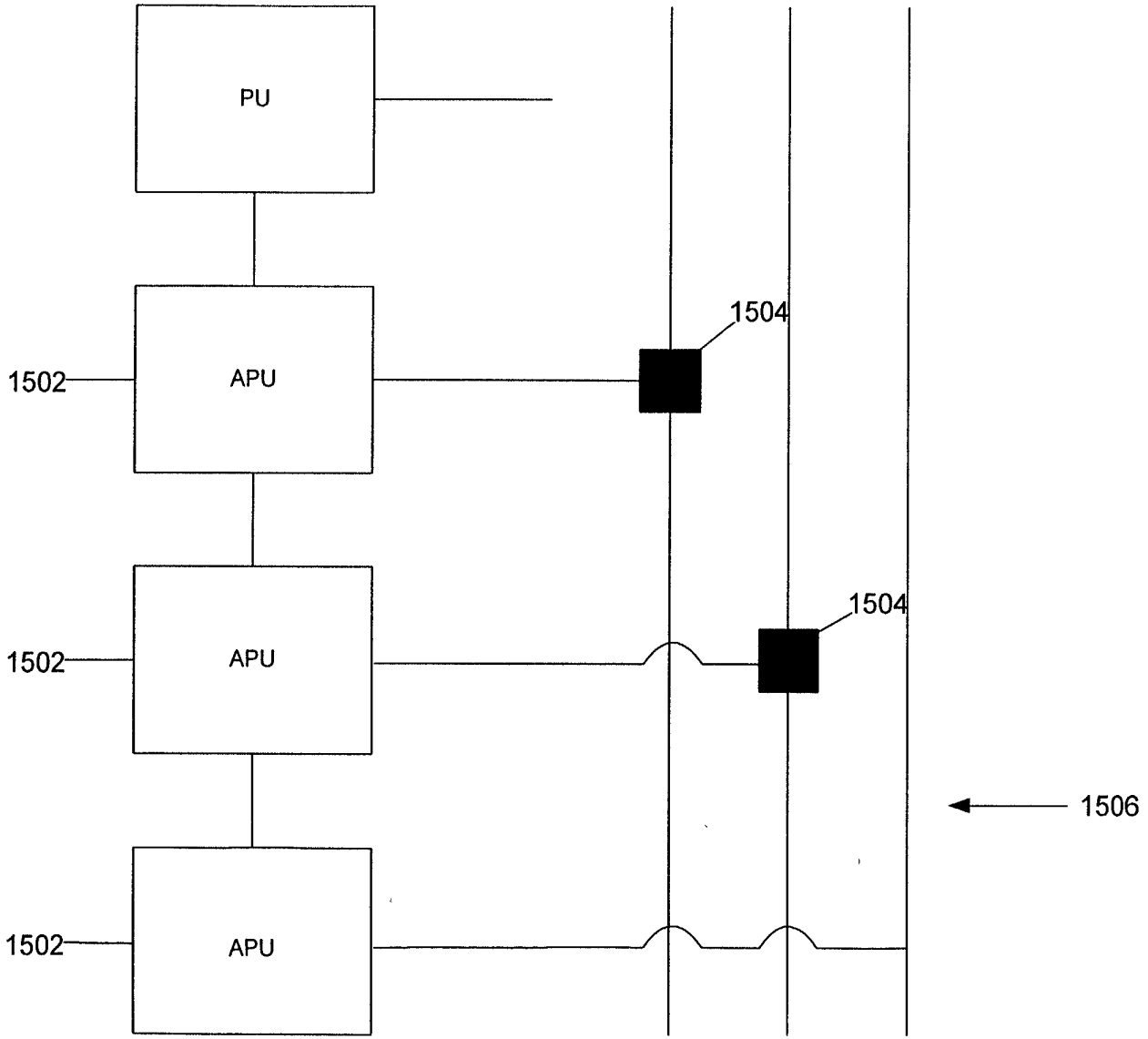

FIG. 15

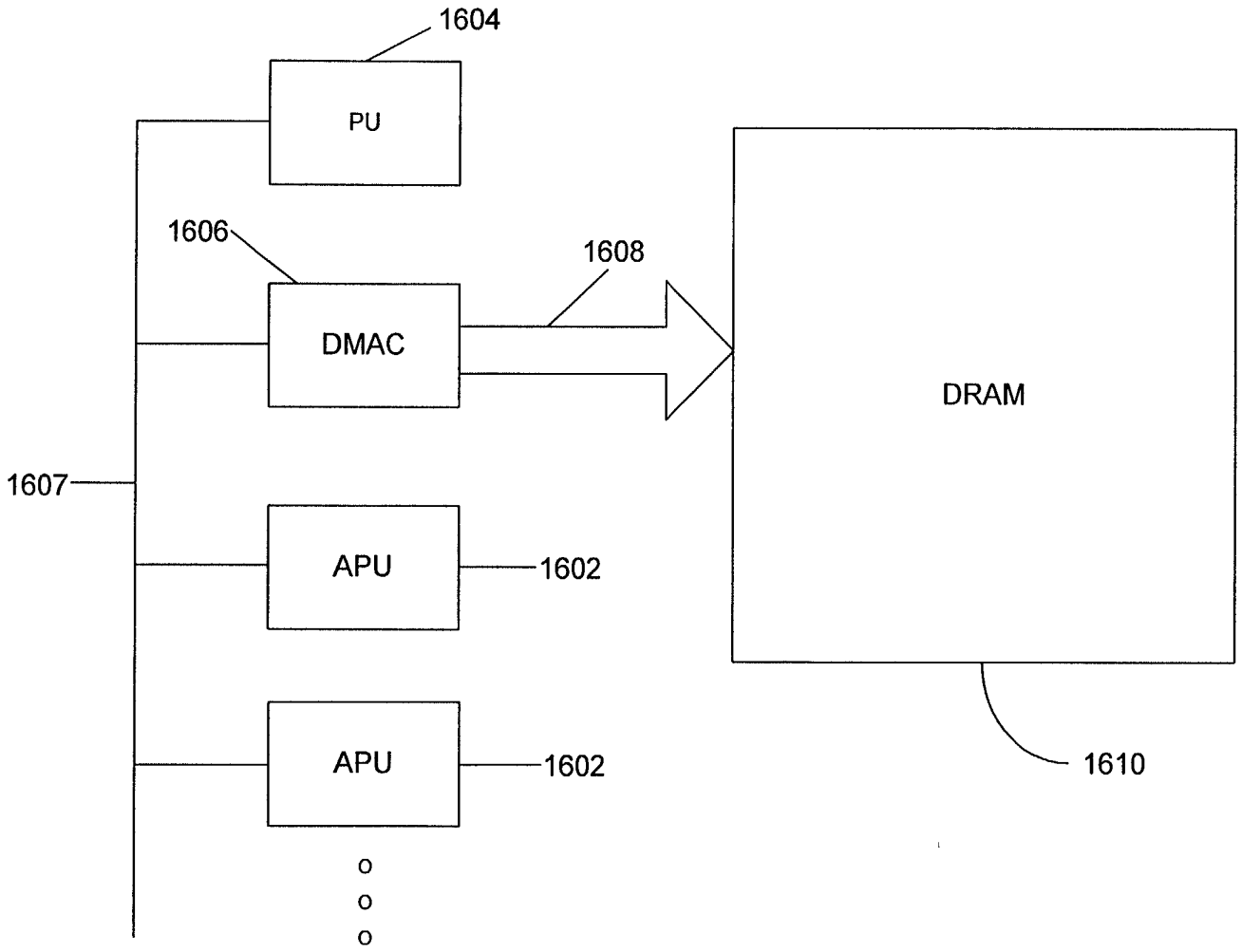

FIG. 16

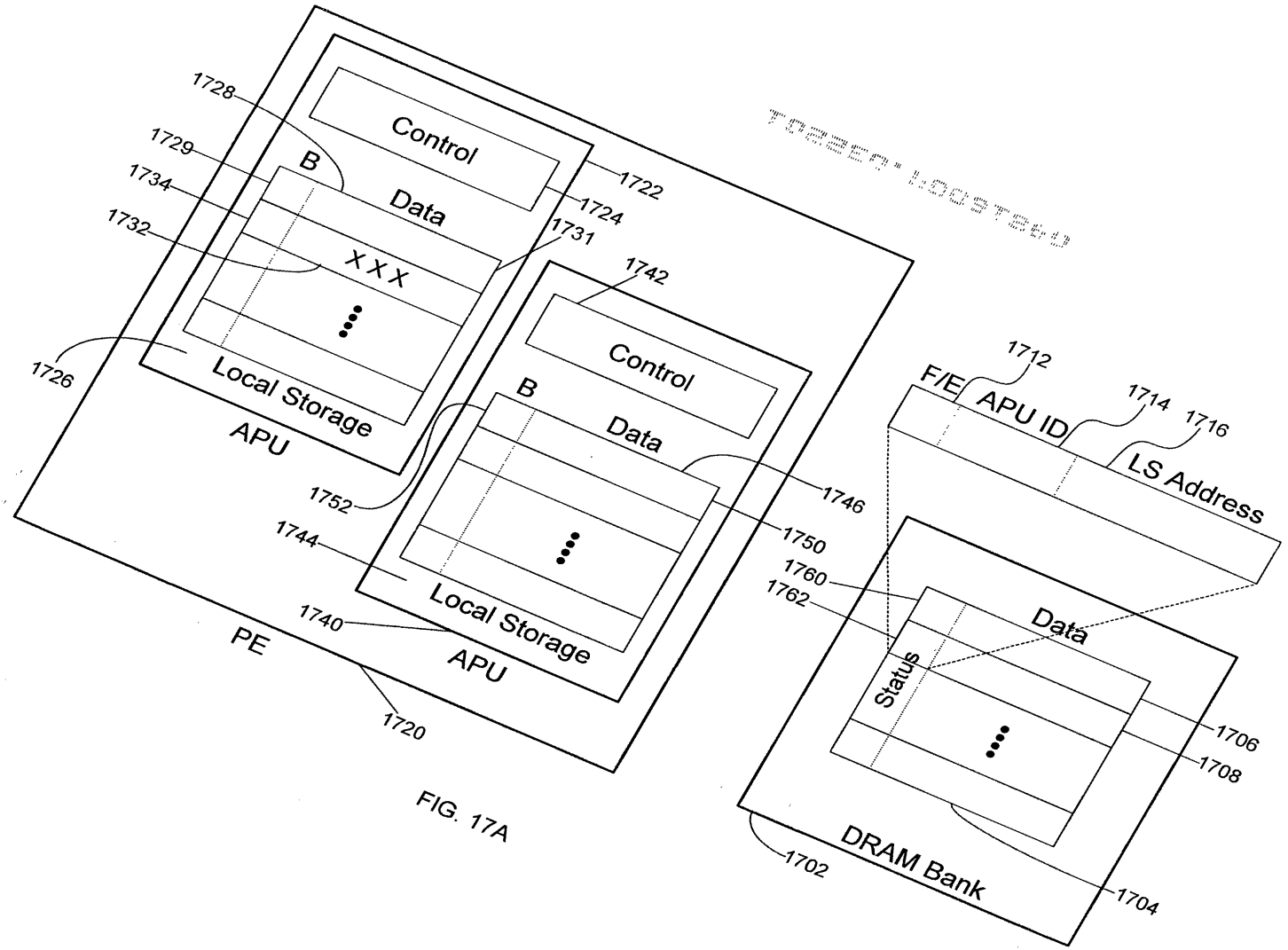
1728
1729
1734
1732
1726
Control
B
Data
XXX
Local Storage
APU
1722
1724
1731
1742
Control
B
Data
1752
1744
1746
1750
Local Storage
APU
1740
PE
1720
1712
F/E
APU ID
1714
1716
LS Address
1760
1762
Data
Status
1706
1708
DRAM Bank
1702
1704

FIG. 17A

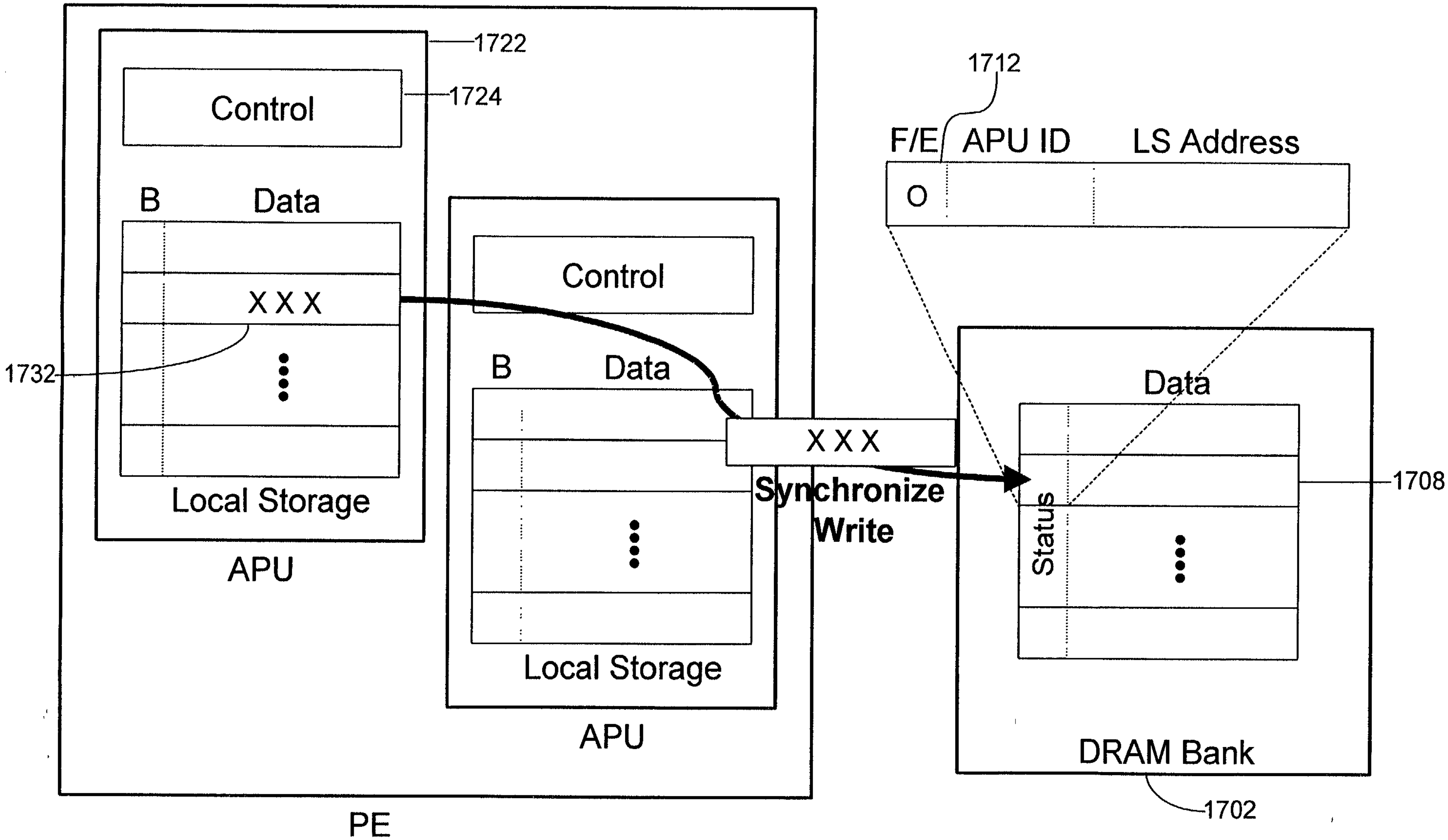

FIG. 17B

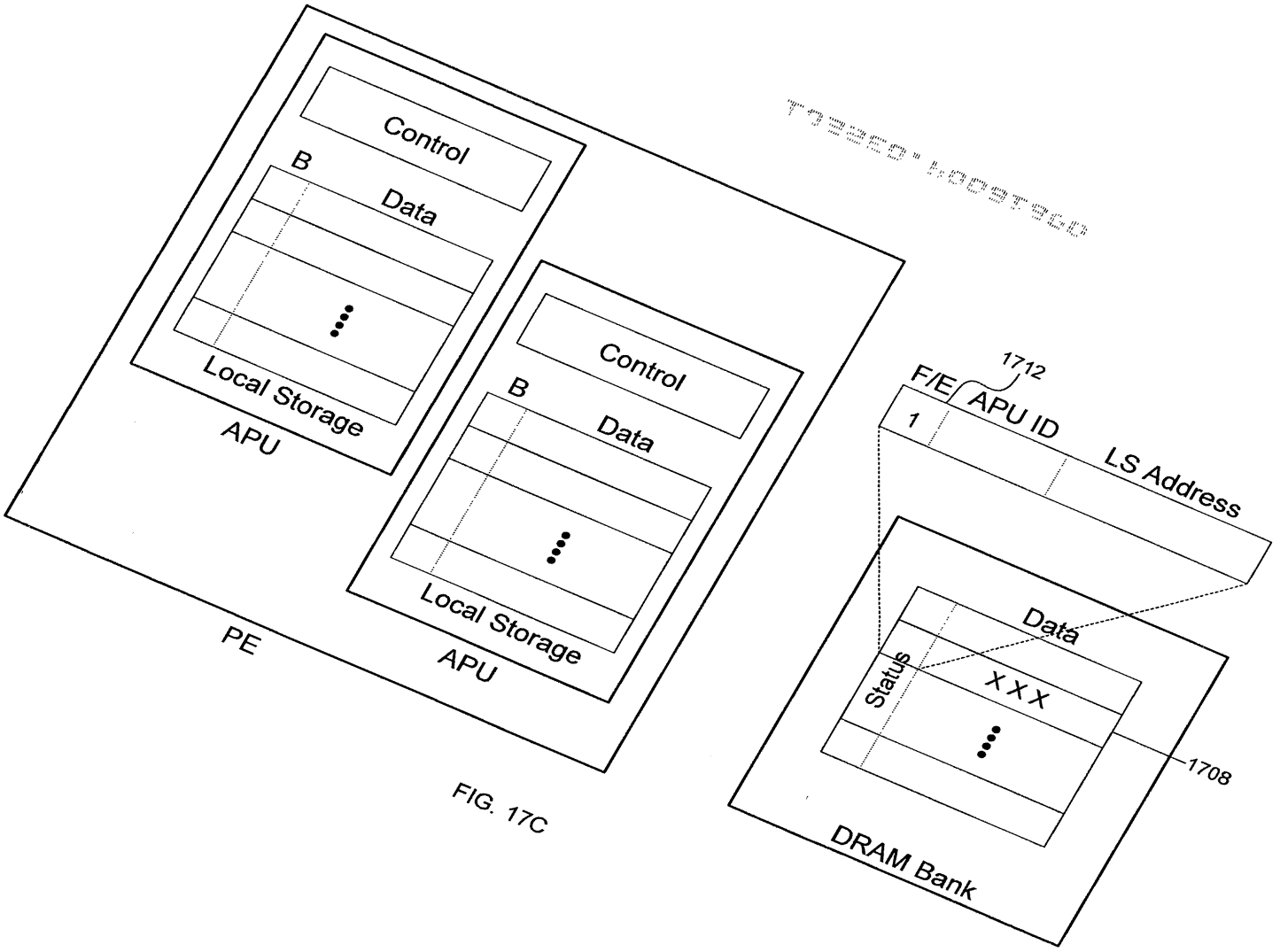
Control
B
Data
Local Storage
APU
Control
B
Data
Local Storage
APU
PE
1712
F/E
APU ID
LS Address
1
Data
Status
XXX
1708
DRAM Bank

FIG. 17C

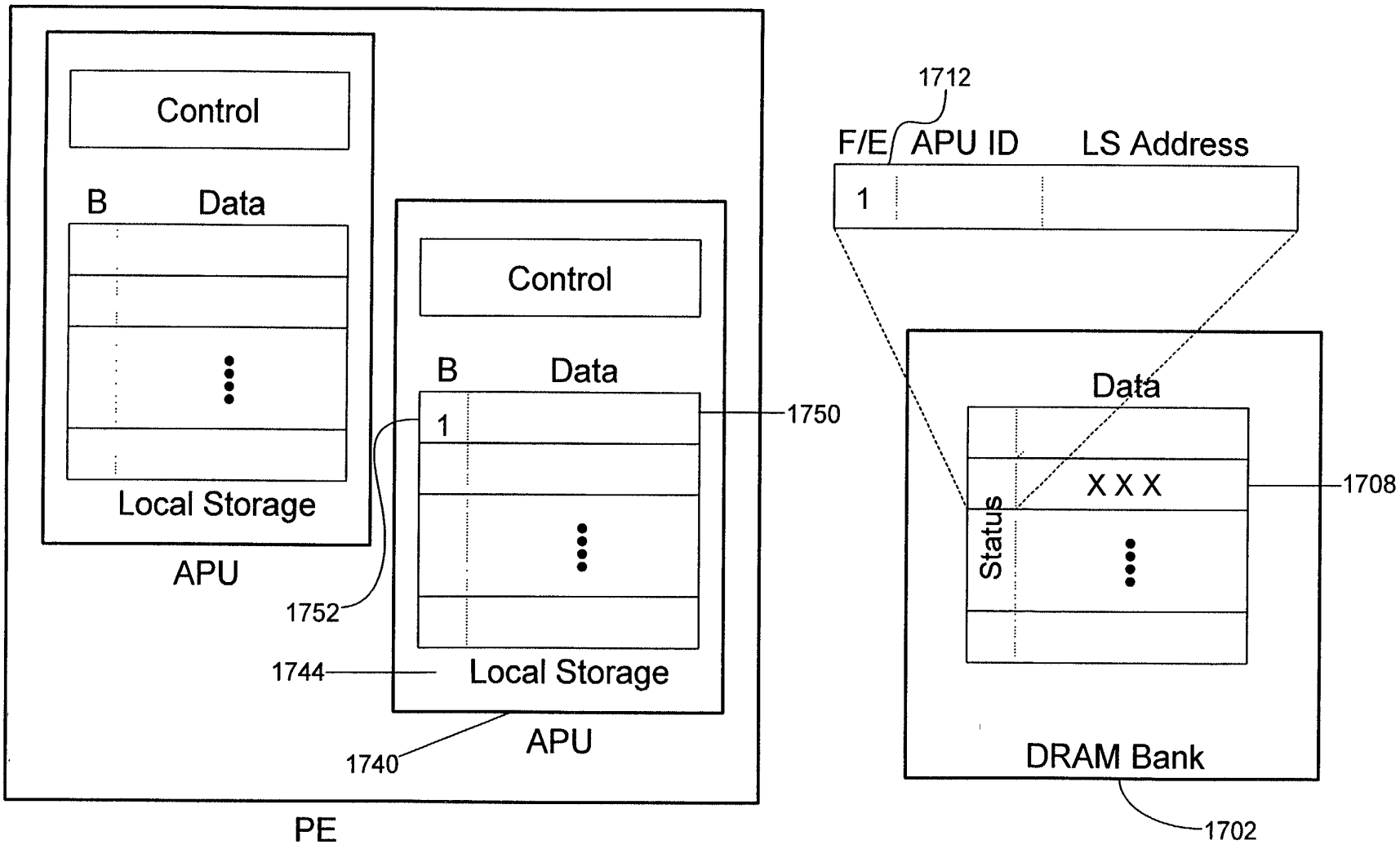
Control
B
Data
Local Storage
APU
Control
B
Data
1
1750
1752
1744
Local Storage
APU
1740
PE
1712
F/E
APU ID
LS Address
1
Data
X X X
Status
1708
DRAM Bank
1702

FIG. 17D

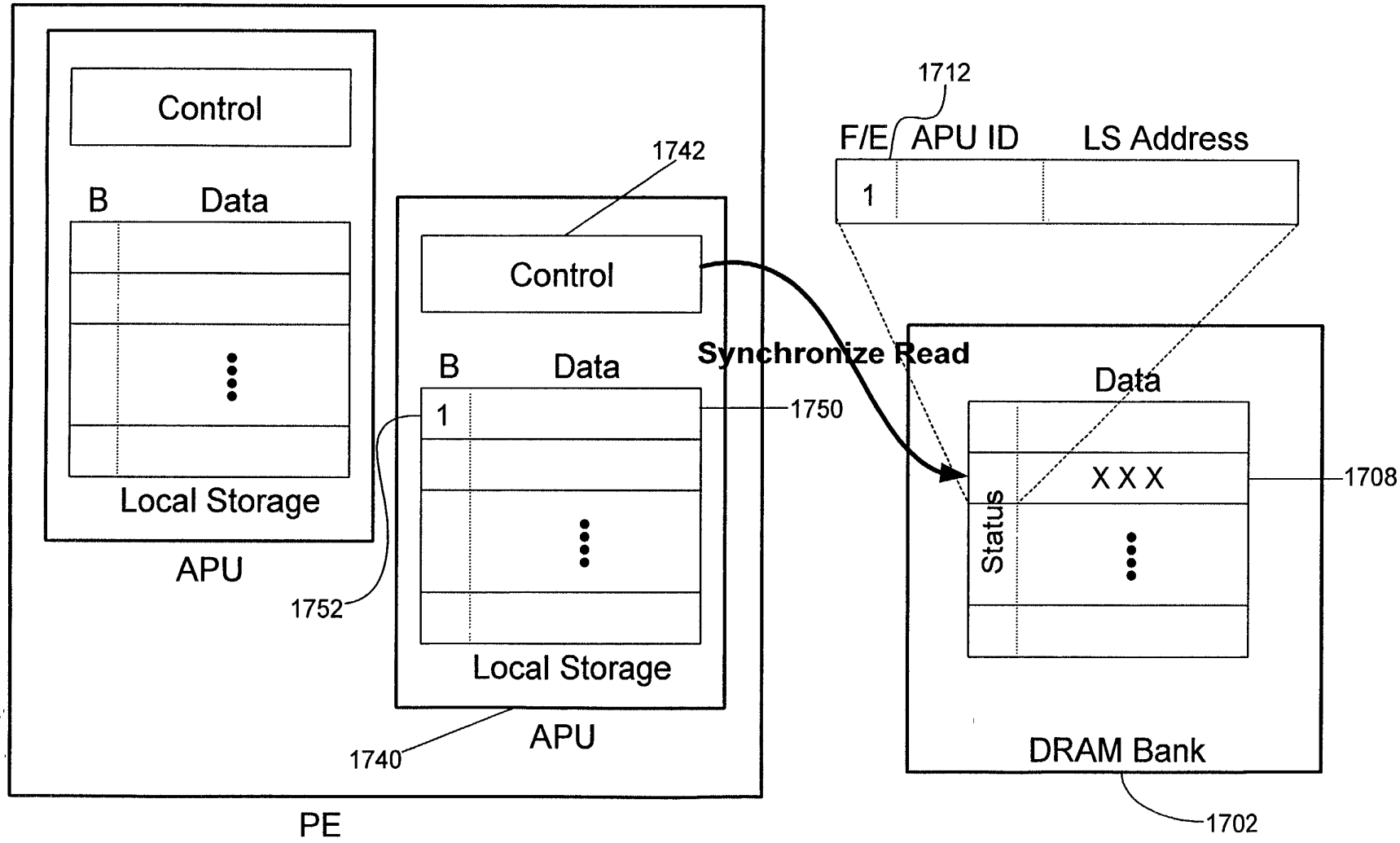
Control
B
Data
Local Storage
APU
1752
1742
Control
B
Data
1
1750
Local Storage
APU
1740
PE
1712
F/E
APU ID
LS Address
1
Synchronize Read
Data
X X X
Status
1708
DRAM Bank
1702

FIG. 17E

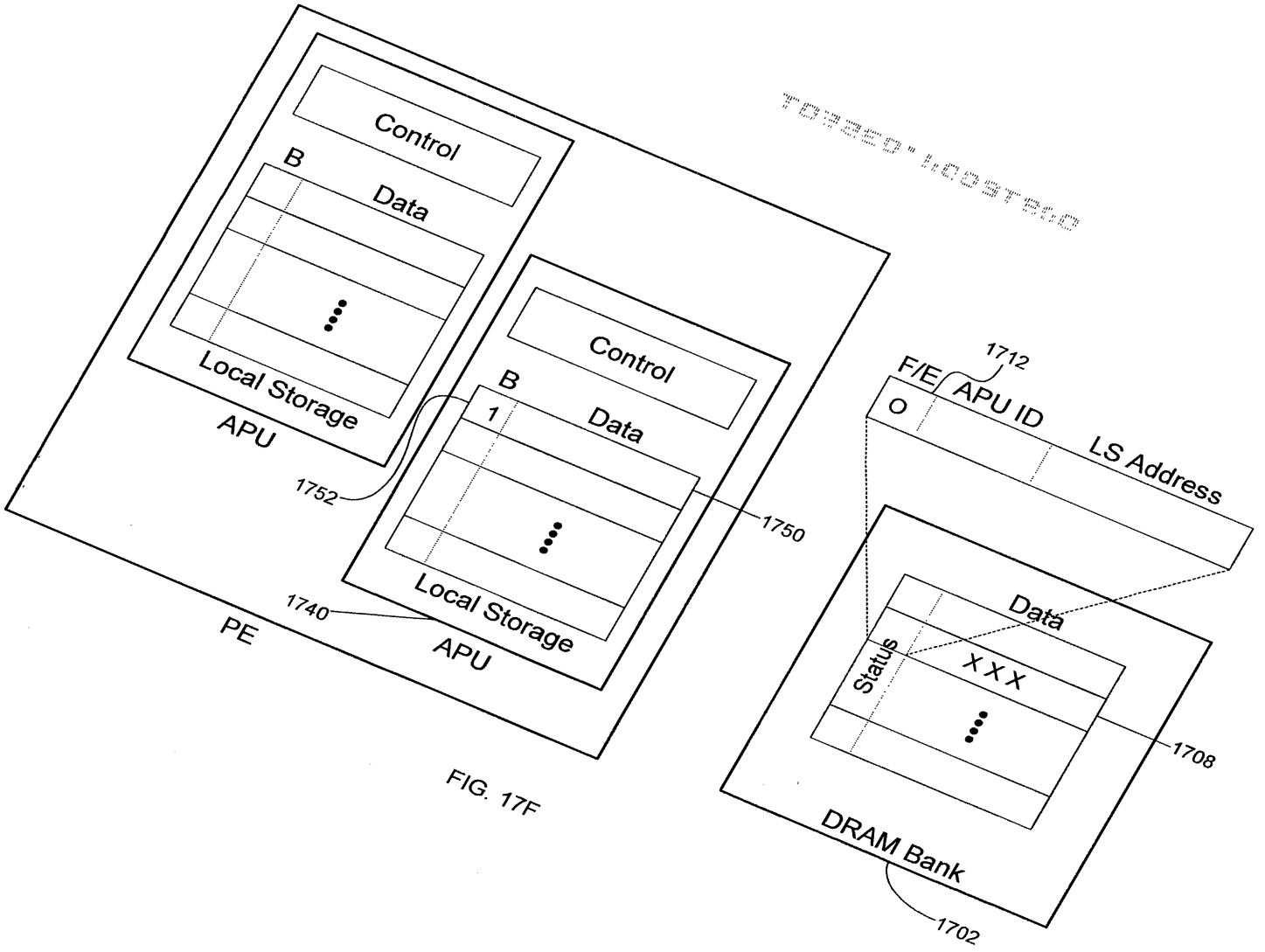
Control
B
Data
Local Storage
APU
1752
Control
B
1
Data
1750
Local Storage
APU
1740
PE
1712
F/E
APU ID
LS Address
O
Data
Status
XXX
1708
DRAM Bank
1702

FIG. 17F

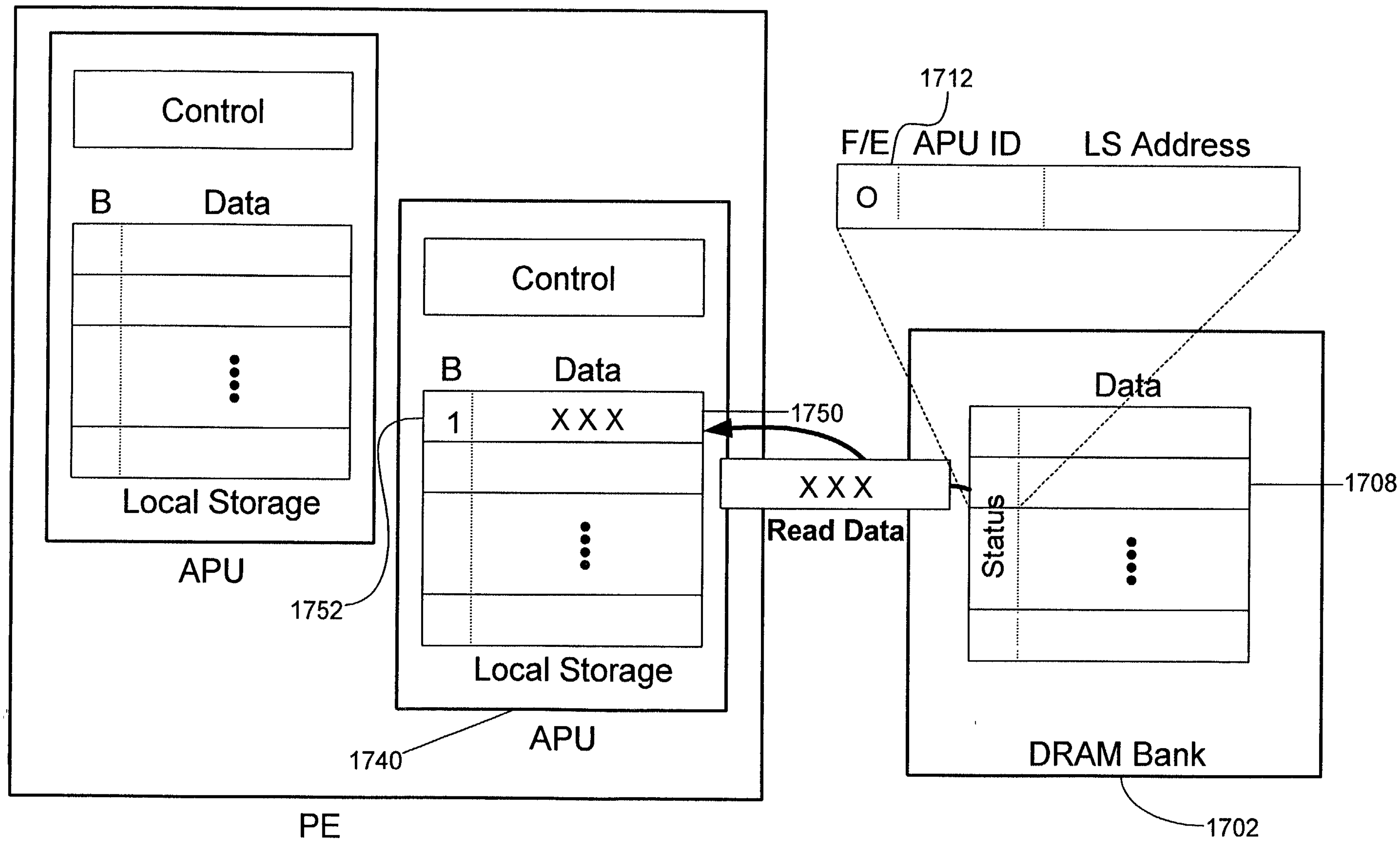

FIG. 17G

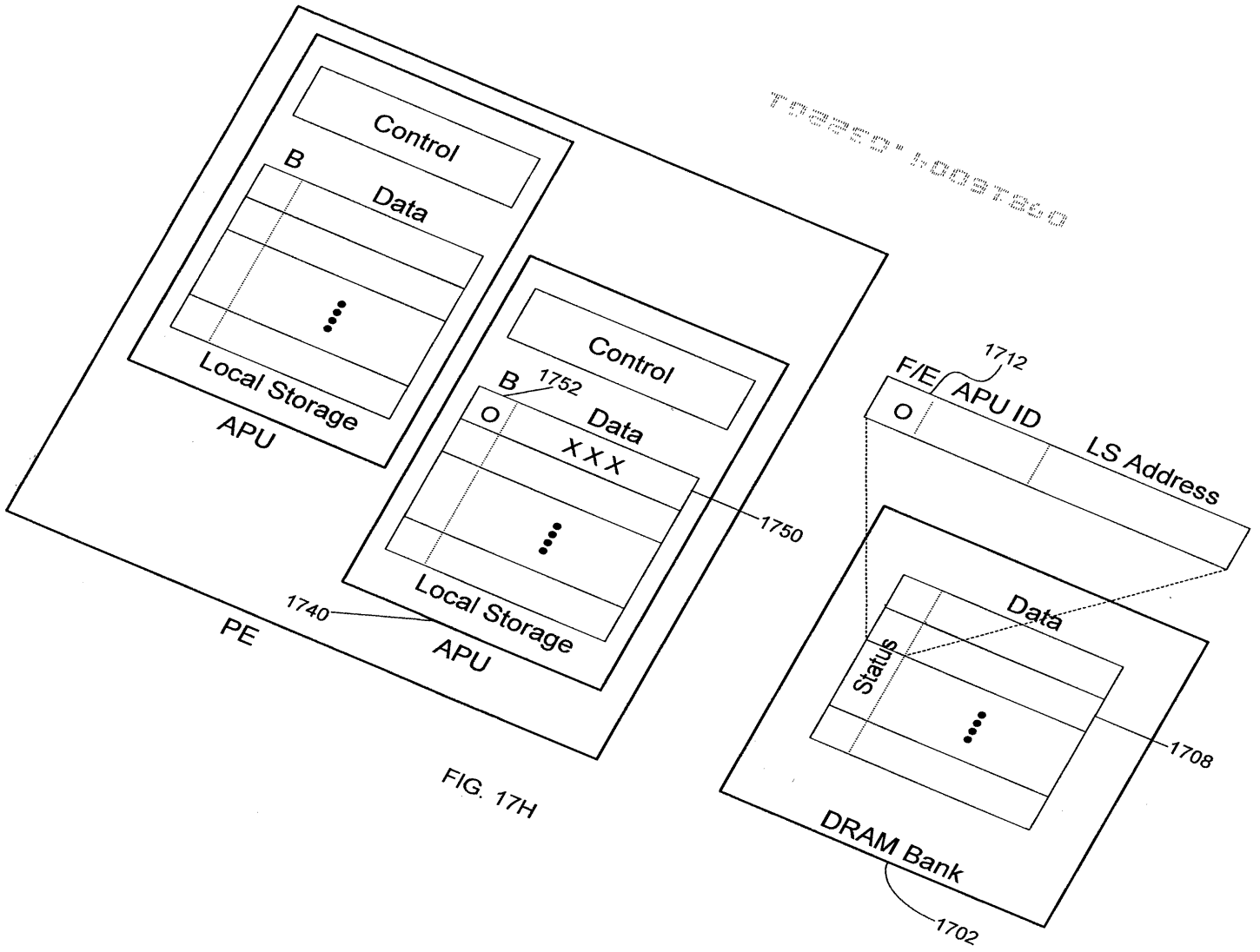
Control
B
Data
Local Storage
APU
Control
B
1752
O
Data
XXX
1750
Local Storage
APU
1740
PE
1712
F/E
APU ID
LS Address
O
Data
Status
1708
DRAM Bank
1702

FIG. 17H

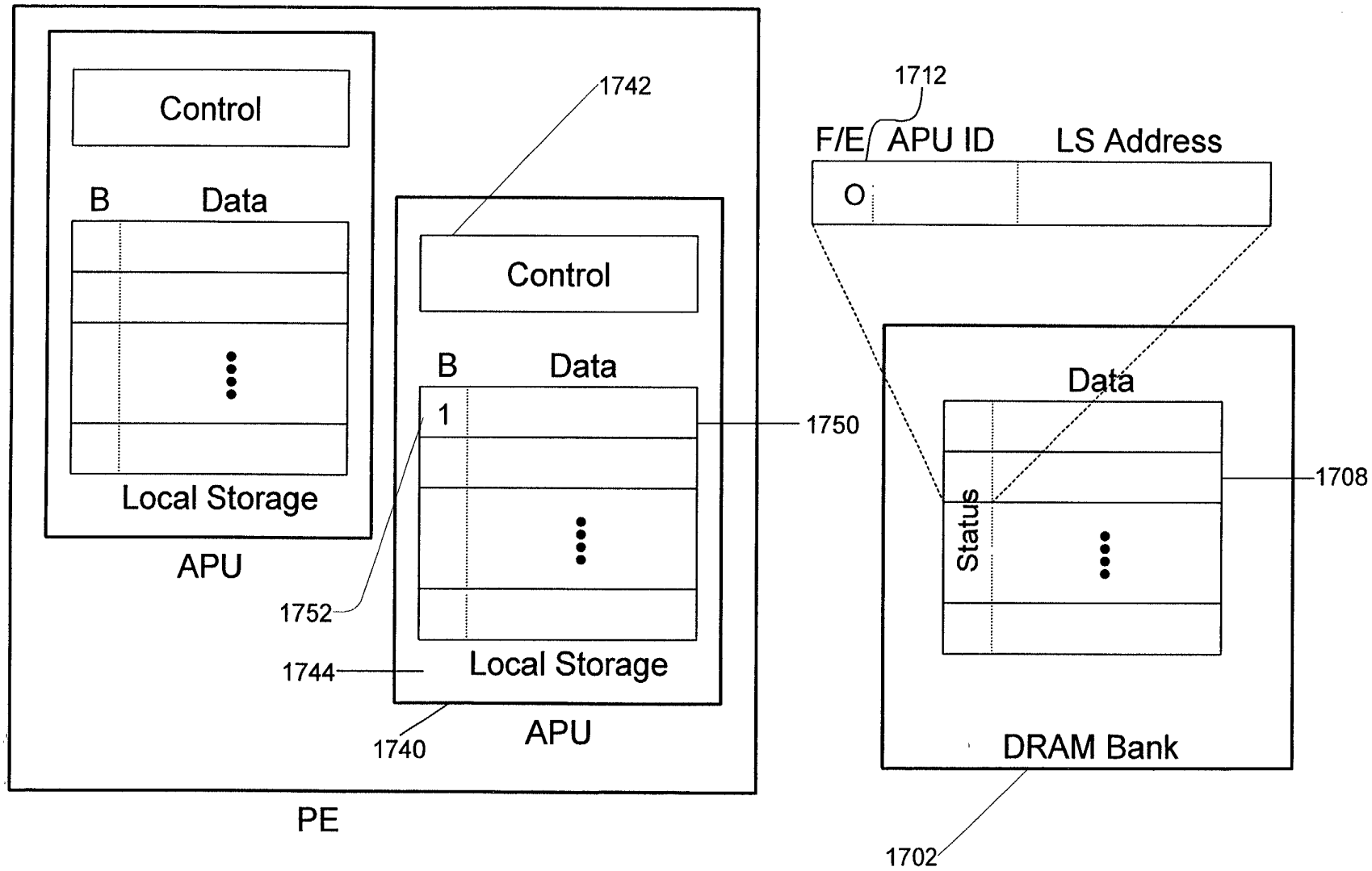

FIG. 17I

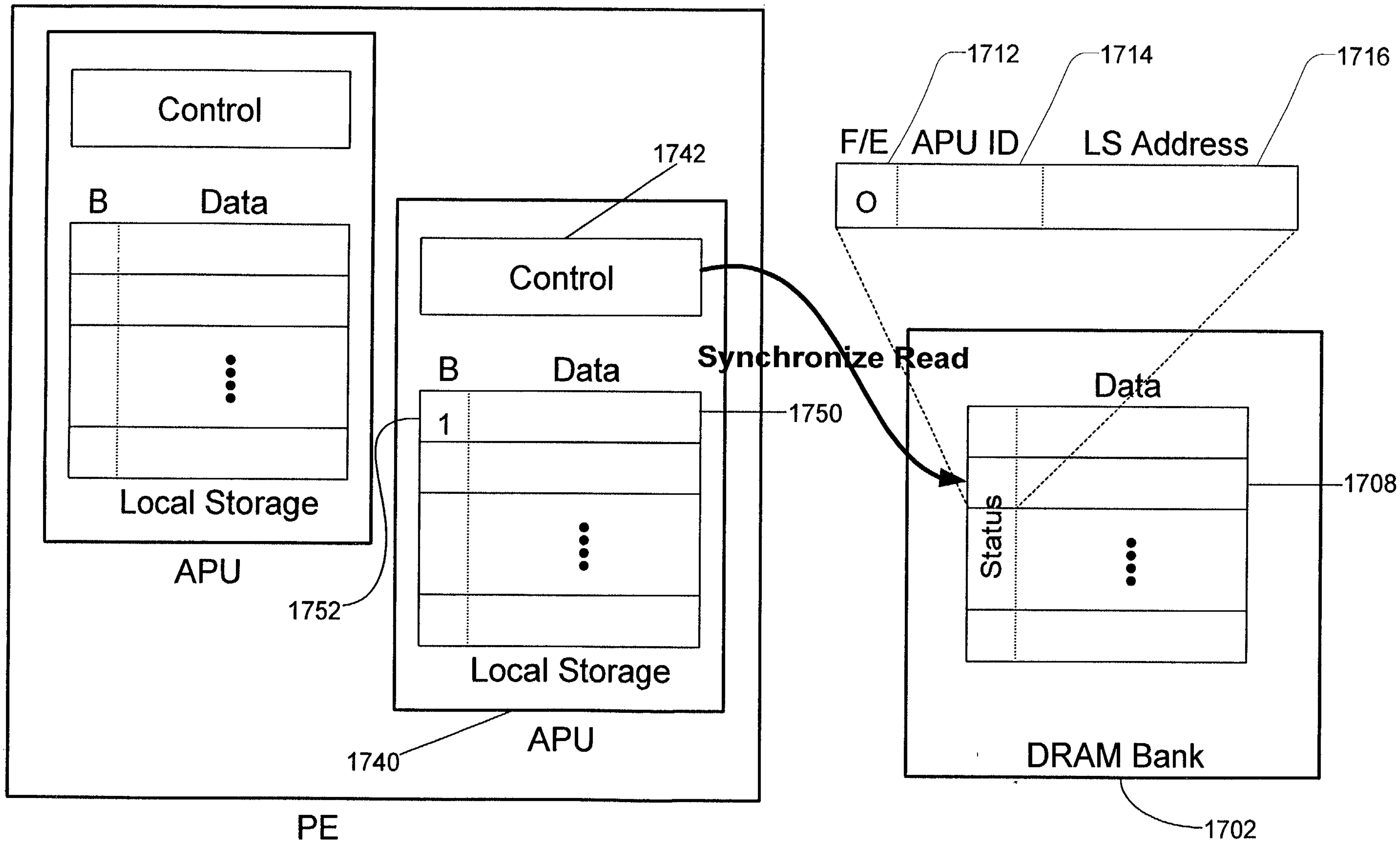

FIG. 17J

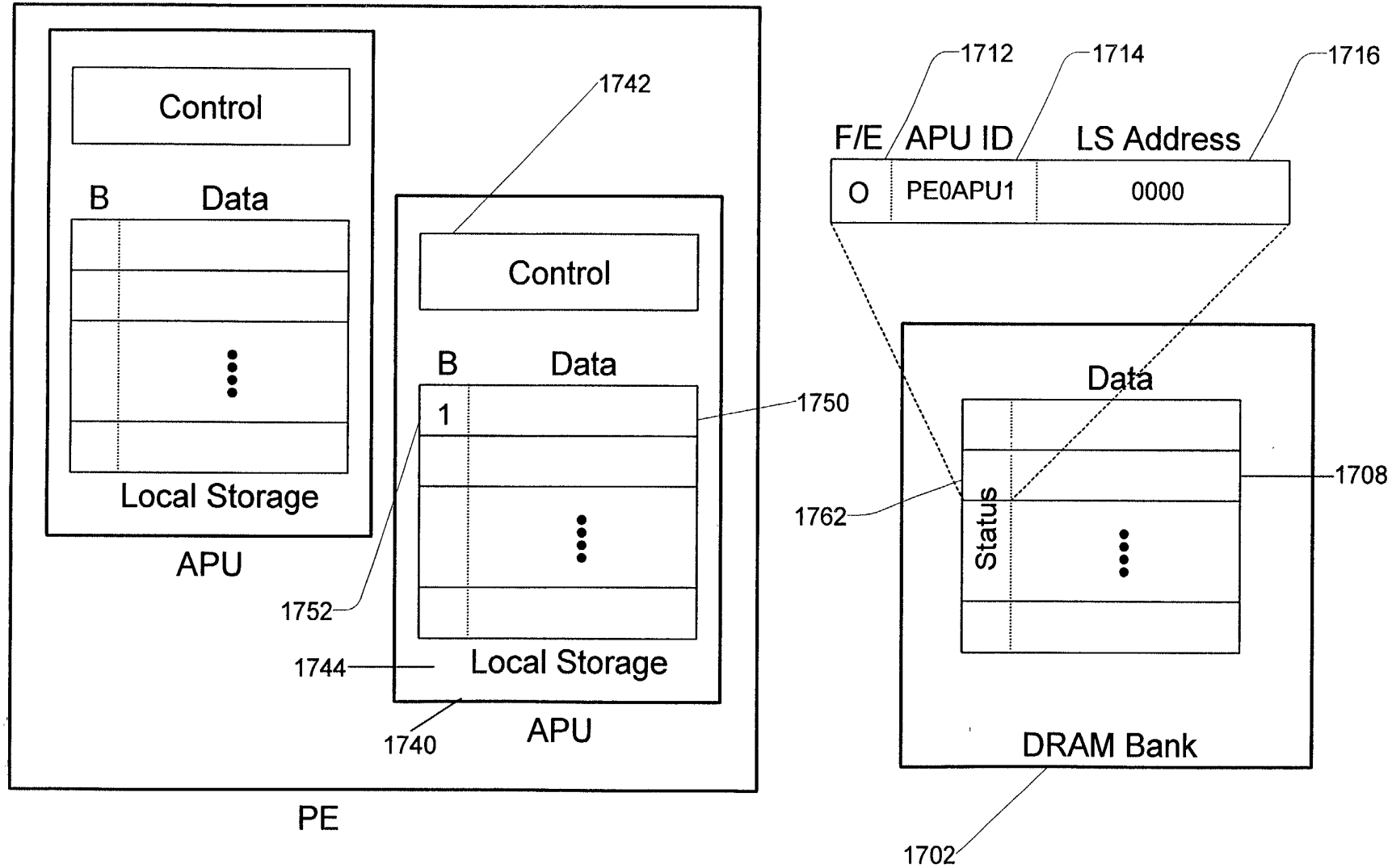
Control
B
Data
Local Storage
APU
1742
Control
B
Data
1
1750
1752
1744
Local Storage
1740
APU
PE
1712
1714
1716
F/E
APU ID
LS Address
O
PE0APU1
0000
Data
1708
1762
Status
DRAM Bank
1702

FIG. 17K

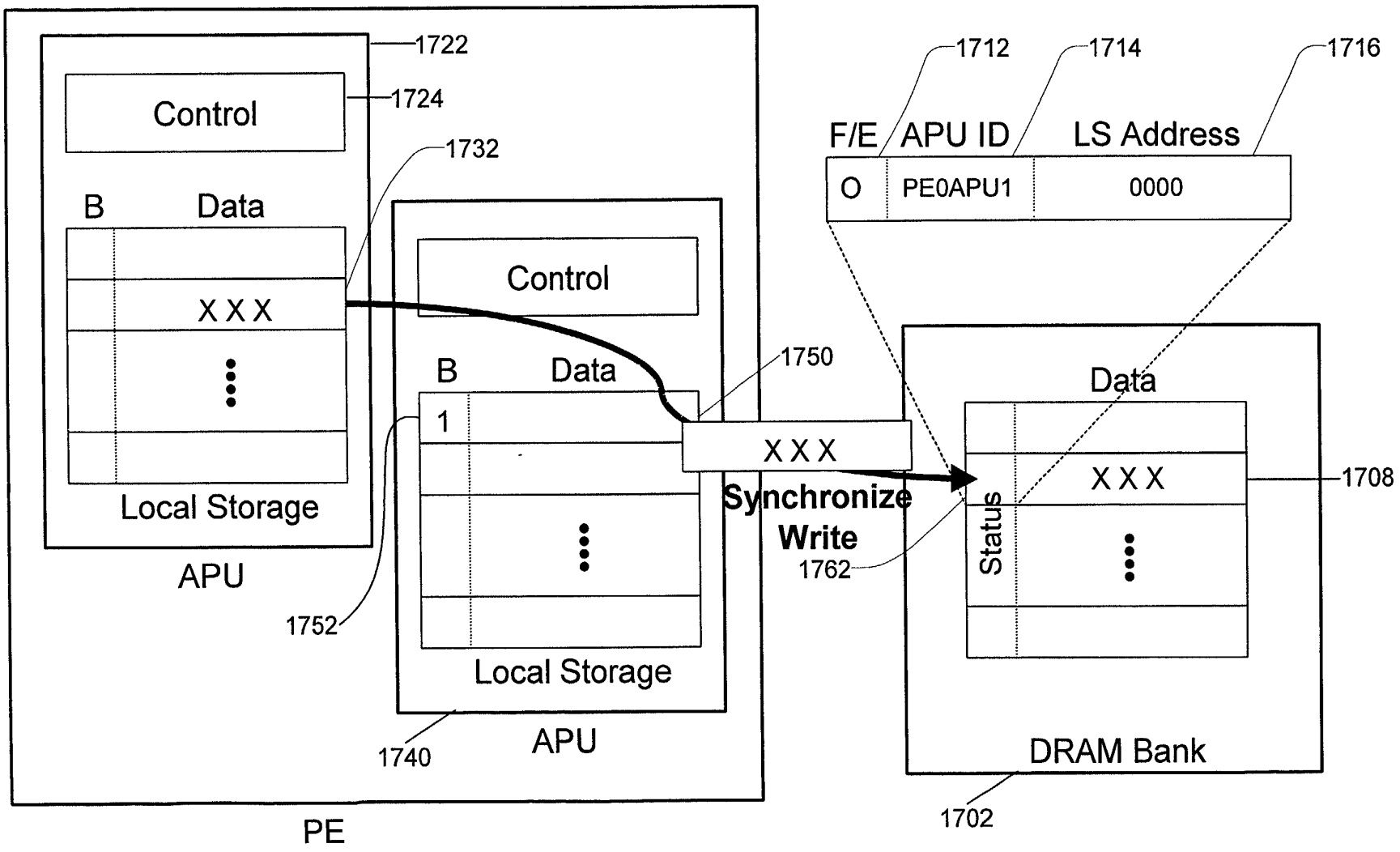

FIG. 17L

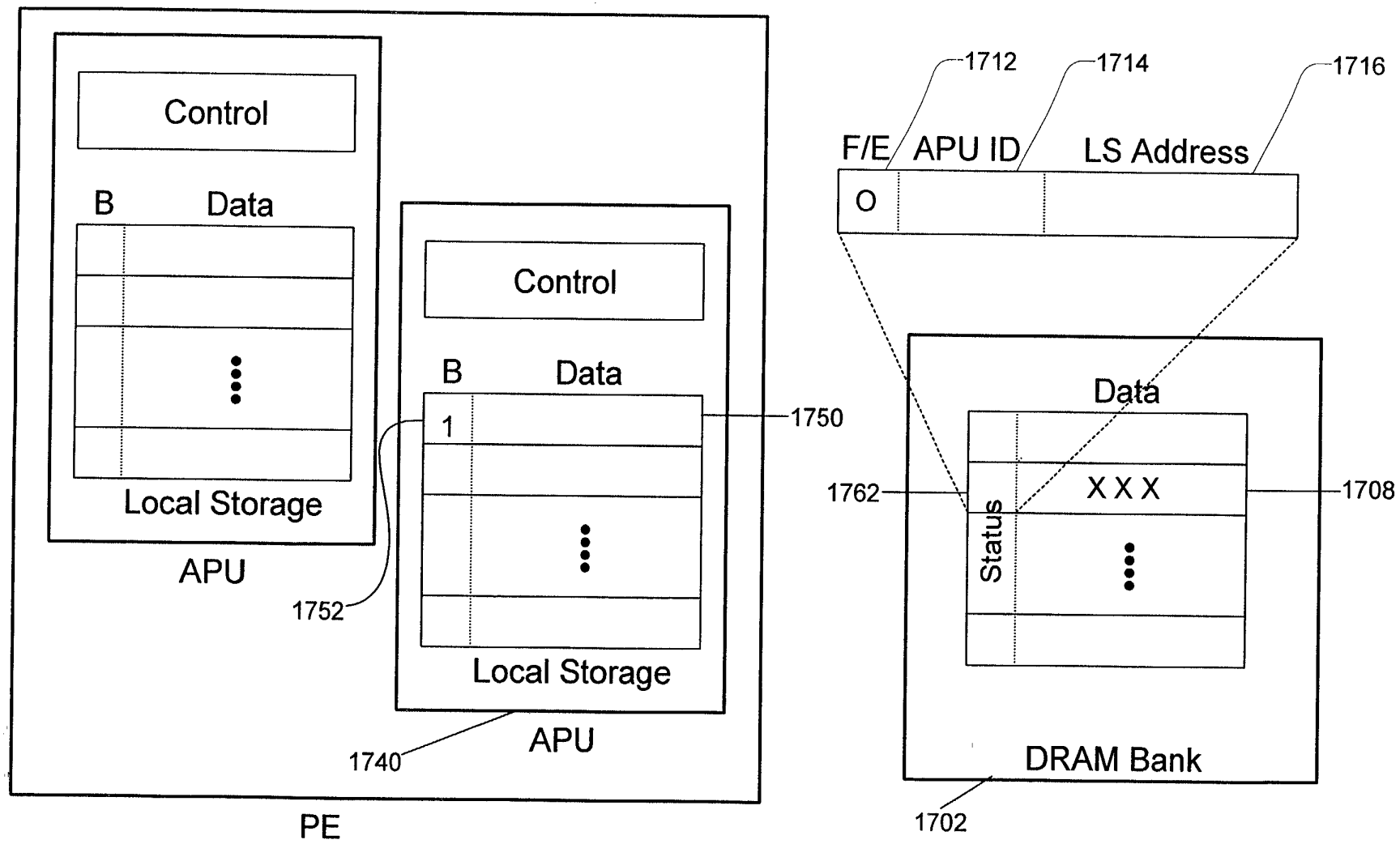

FIG. 17M

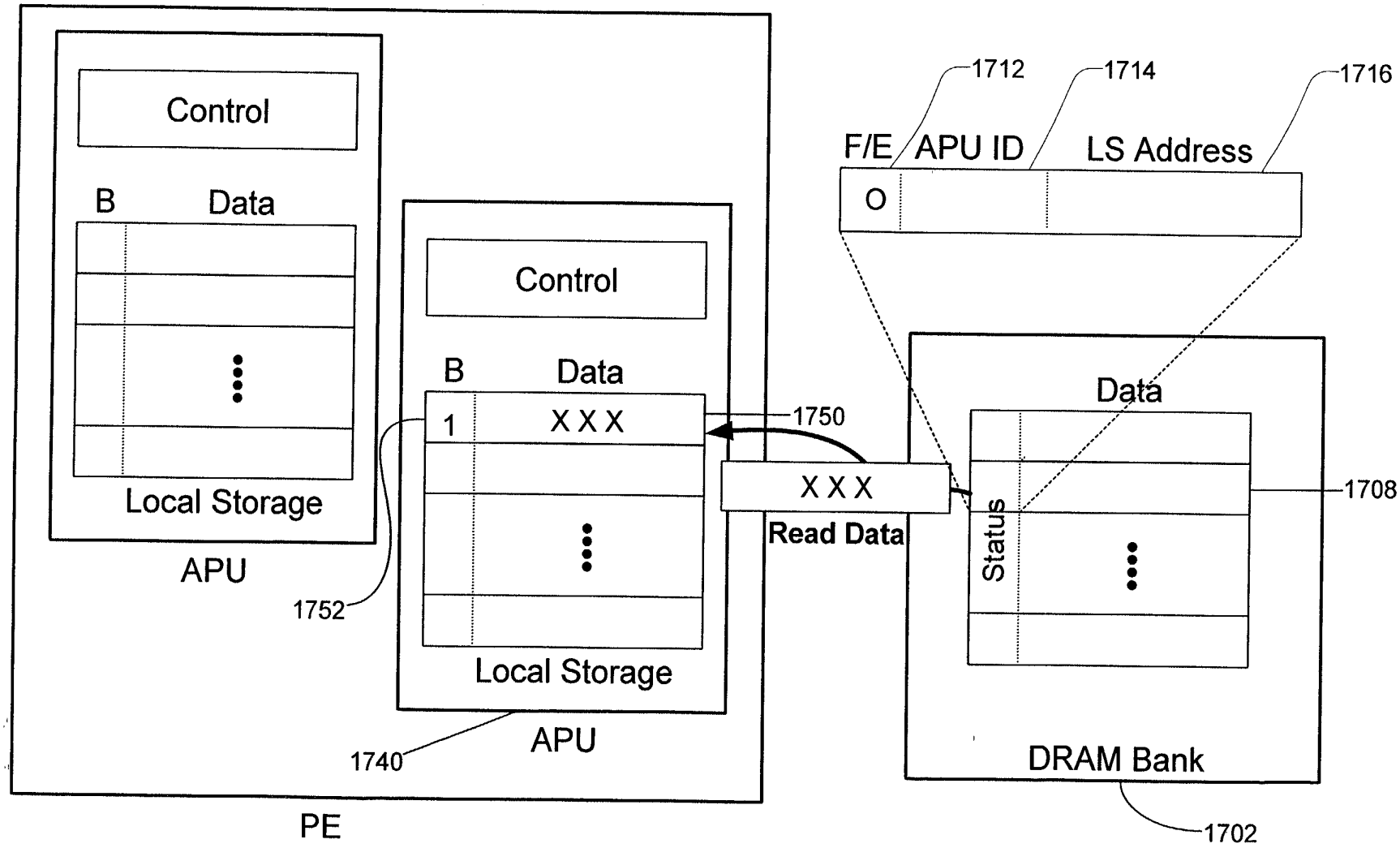
Control
B
Data
Local Storage
APU
Control
B
Data
1
X X X
1750
1752
Local Storage
APU
1740
PE
1712
1714
1716
F/E
APU ID
LS Address
0
X X X
Read Data
Data
Status
1708
DRAM Bank
1702

FIG. 17N

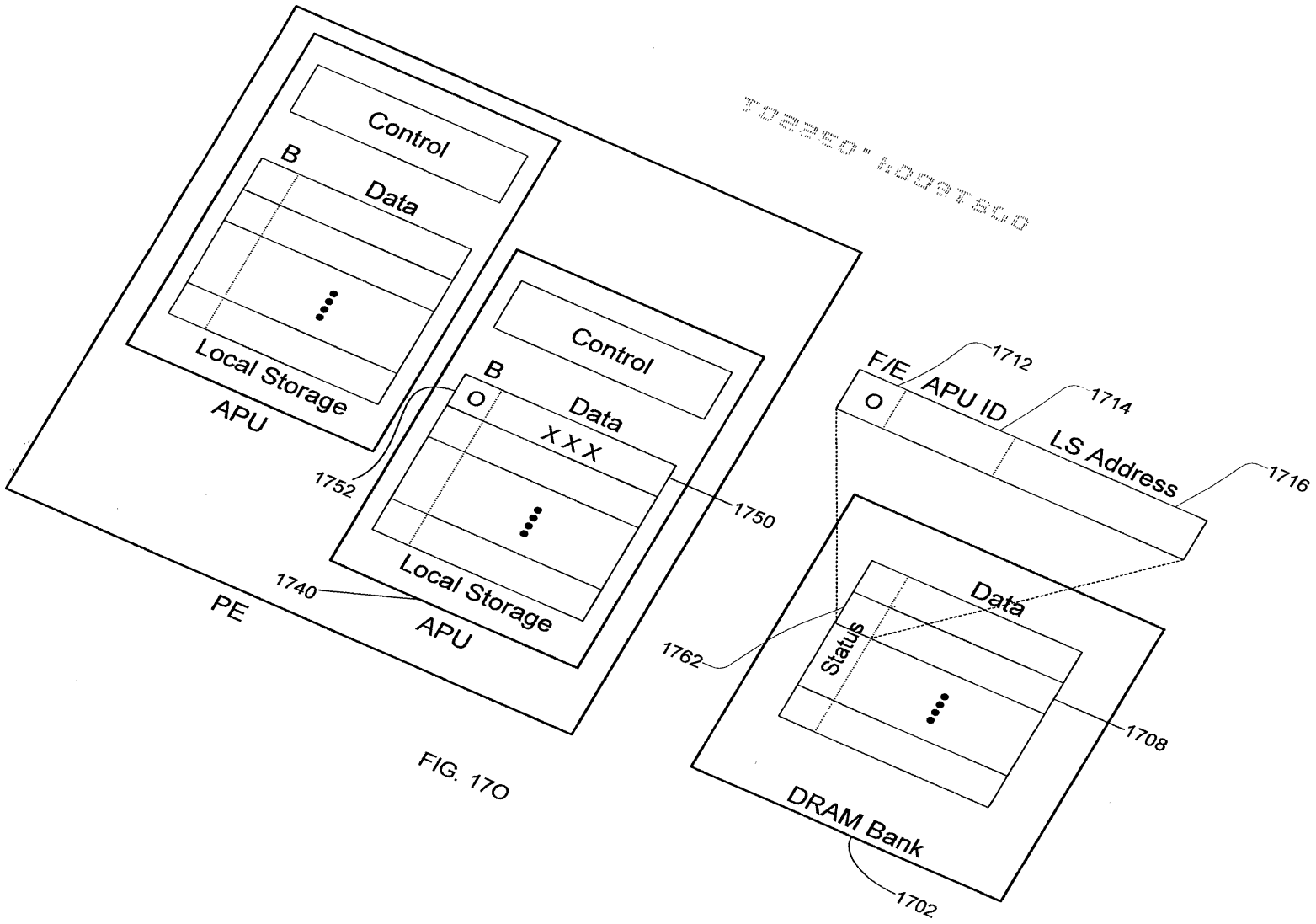
Control
B
Data
Local Storage
APU
Control
B
O
Data
XXX
Local Storage
APU
PE
1740
1750
1752
F/E
O
APU ID
LS Address
1712
1714
1716
Data
Status
1762
1708
DRAM Bank
1702

FIG. 17O

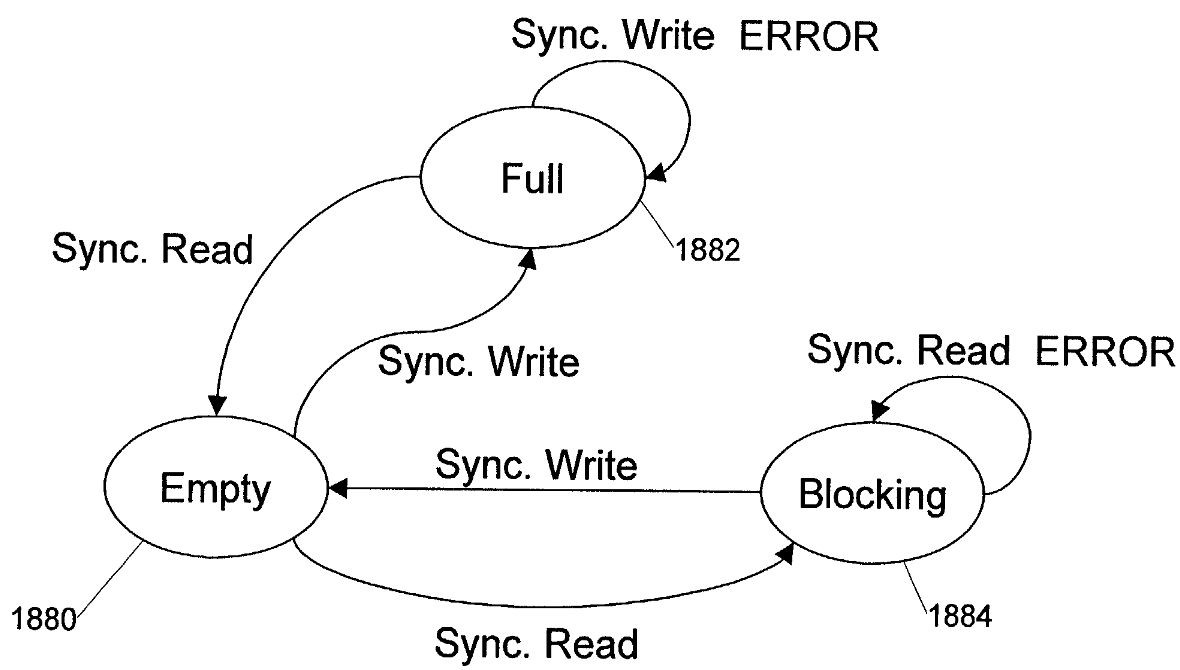

FIG. 18

Key Control Table

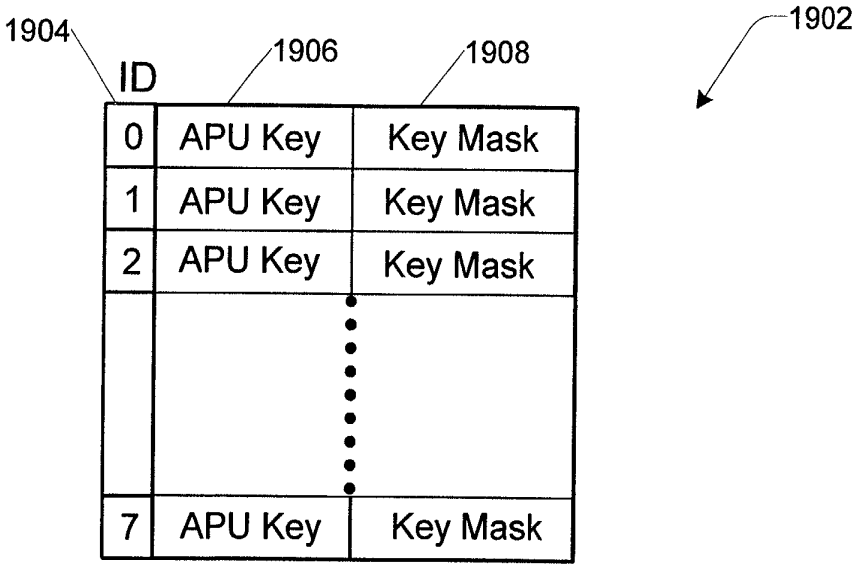

FIG. 19

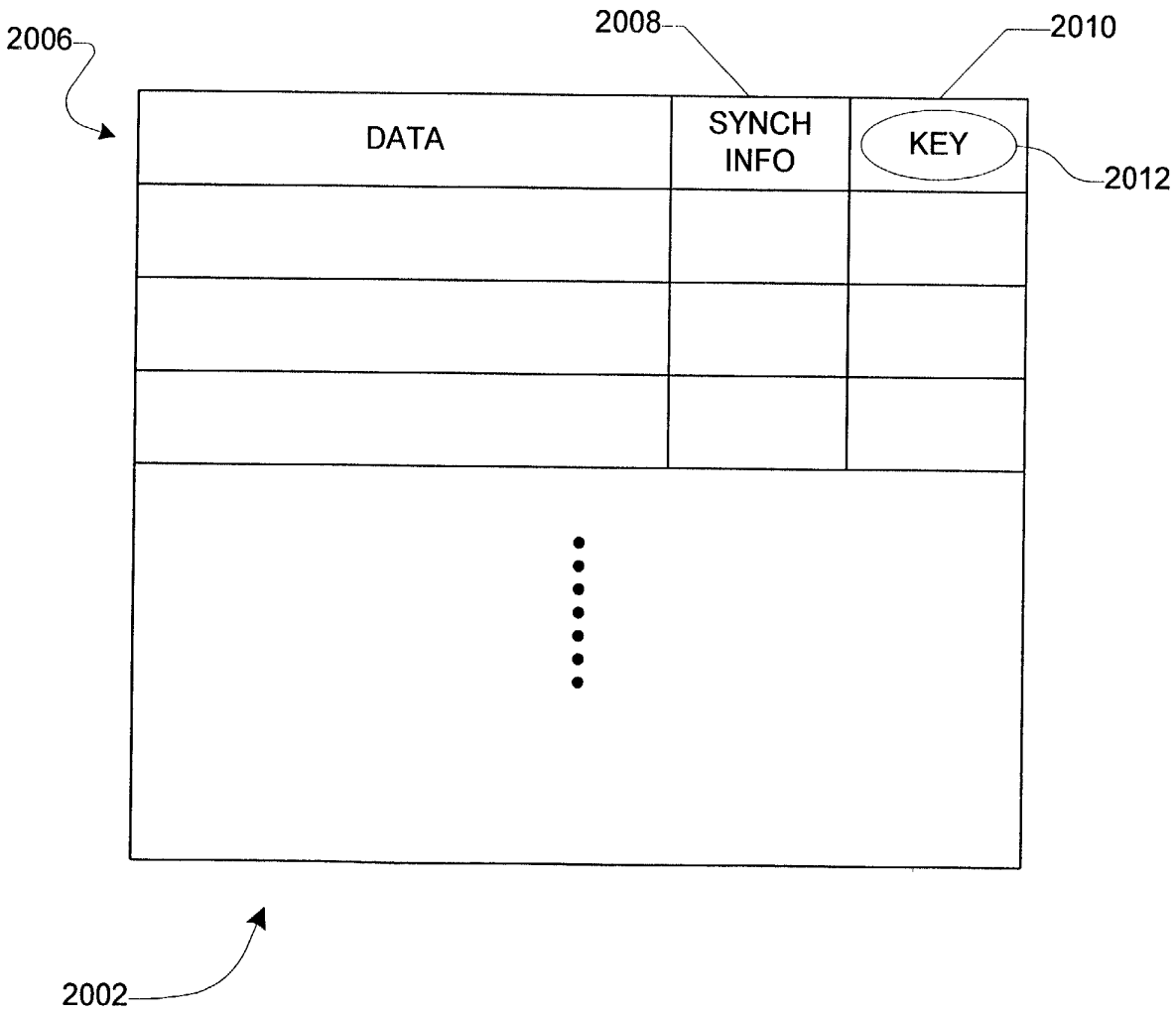

FIG. 20

Memory Access Control Table

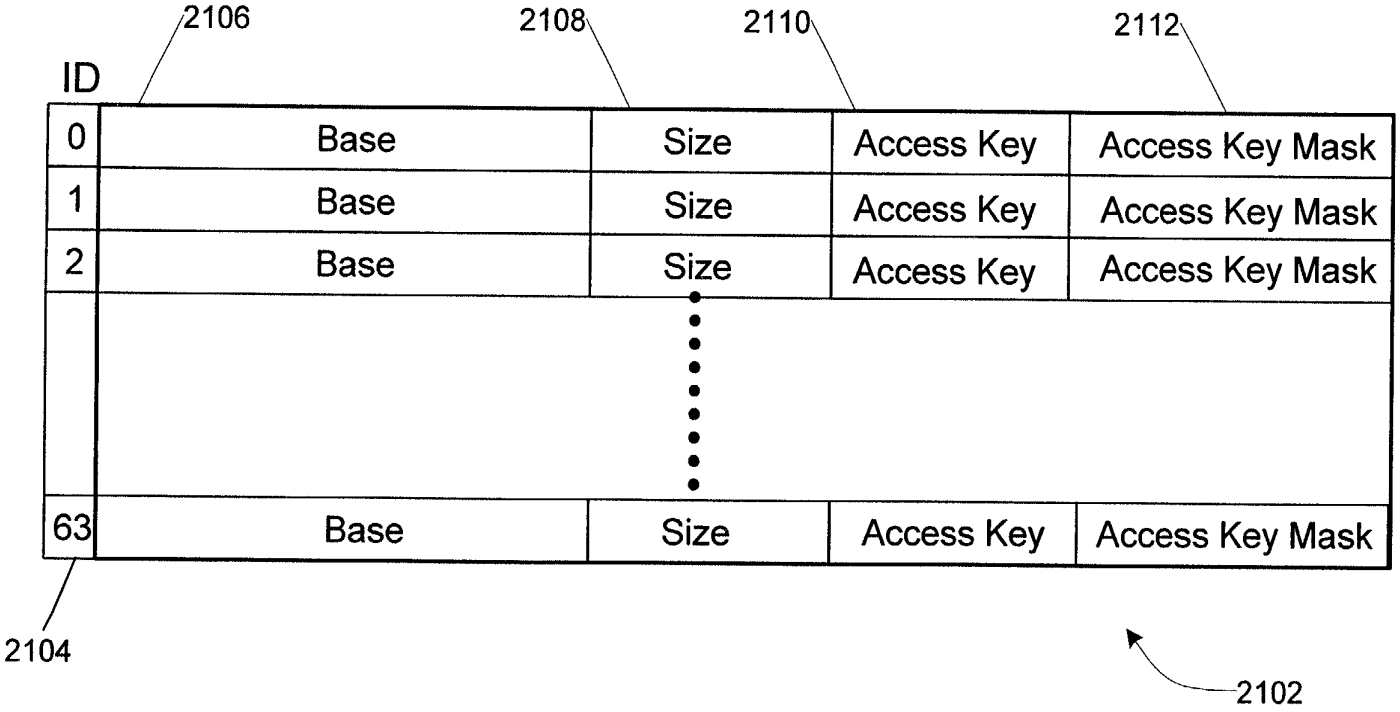

FIG. 21

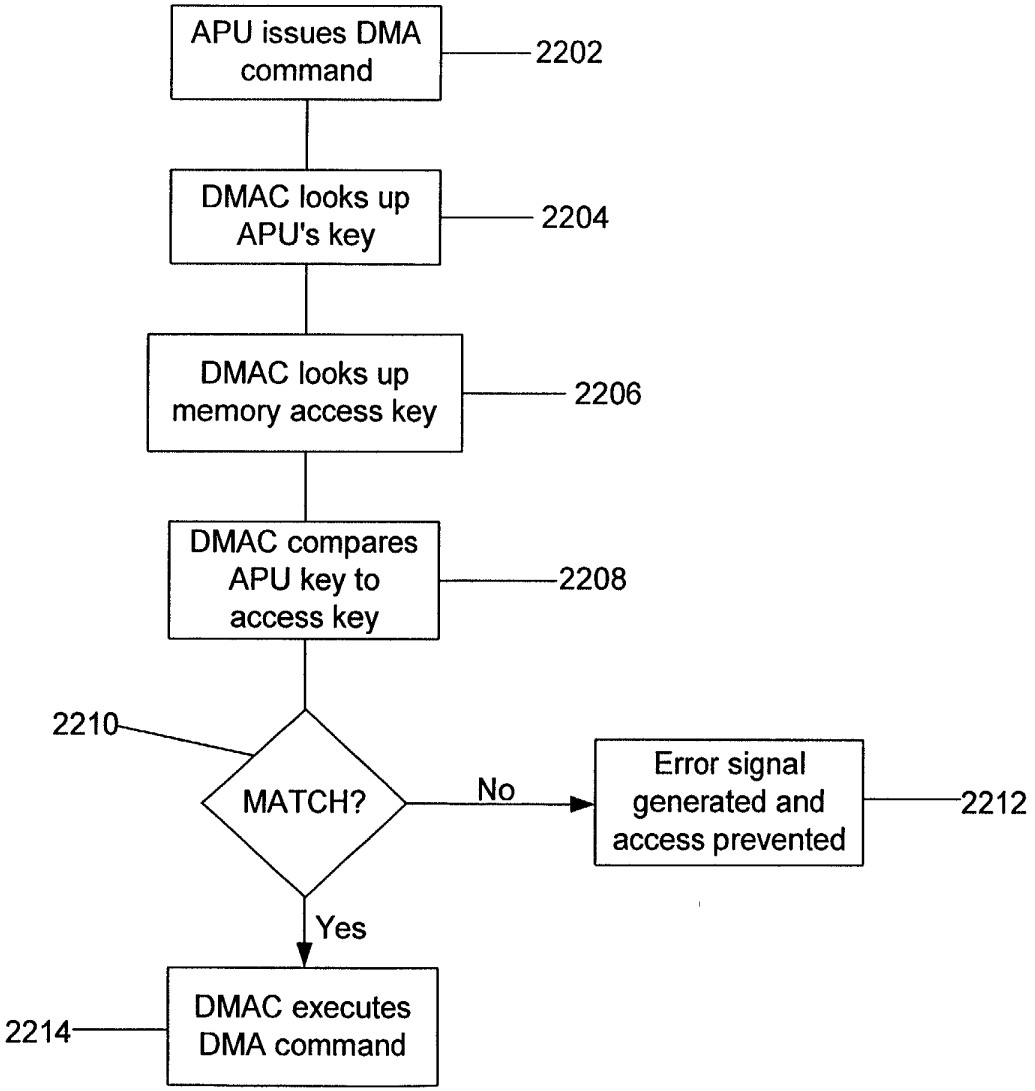

FIG. 22

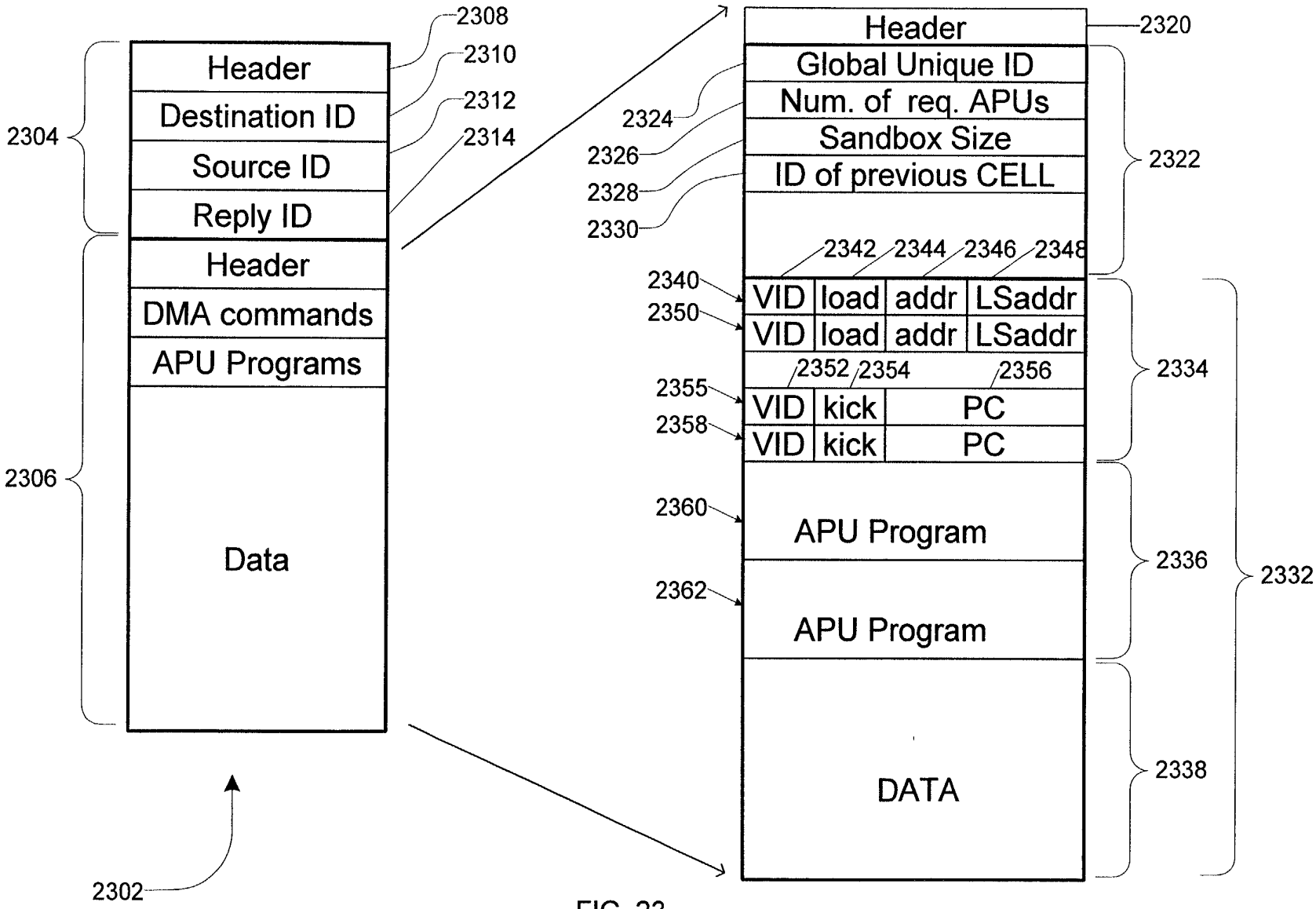
2308
2310
2312
2314
2304
Header
Destination ID
Source ID
Reply ID
Header
DMA commands
APU Programs
Data
2306
2302
2320
Header
Global Unique ID
Num. of req. APUs
Sandbox Size
ID of previous CELL
2324
2326
2328
2330
2322
2342
2344
2346
2348
2340
2350
VID
load
addr
LSaddr
VID
load
addr
LSaddr
2352
2354
2356
2355
2358
VID
kick
PC
VID
kick
PC
2334
2360
APU Program
2362
APU Program
2336
2332
DATA
2338

FIG. 23

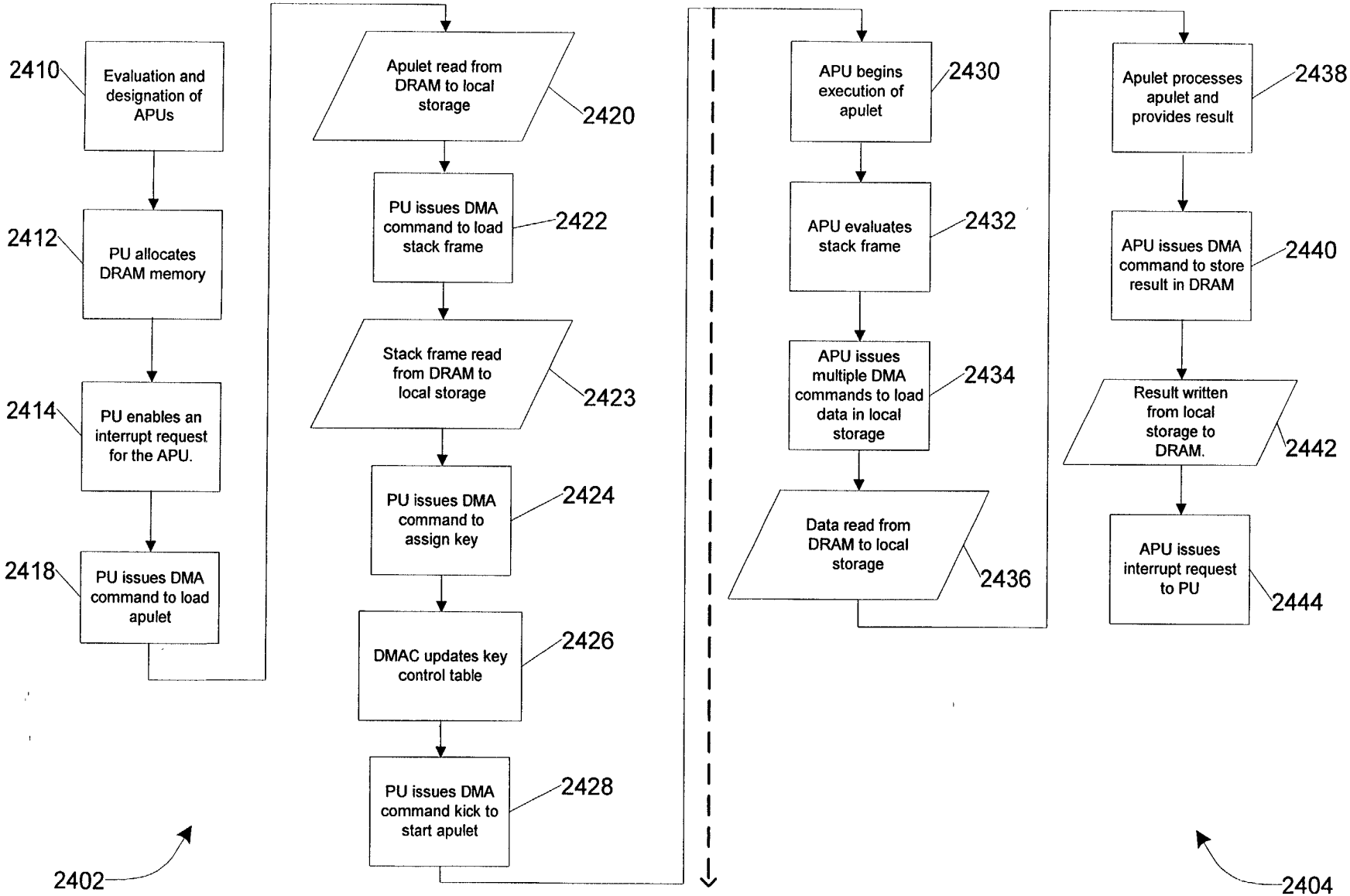
2410
Evaluation and designation of APUs
2412
PU allocates DRAM memory
2414
PU enables an interrupt request for the APU.
2418
PU issues DMA command to load apulet
Apulet read from DRAM to local storage
2420
PU issues DMA command to load stack frame
2422
Stack frame read from DRAM to local storage
2423
PU issues DMA command to assign key
2424
DMAC updates key control table
2426
PU issues DMA command kick to start apulet
2428
APU begins execution of apulet
2430
APU evaluates stack frame
2432
APU issues multiple DMA commands to load data in local storage
2434
Data read from DRAM to local storage
2436
Apulet processes apulet and provides result
2438
APU issues DMA command to store result in DRAM
2440
Result written from local storage to DRAM.
2442
APU issues interrupt request to PU
2444
2402
2404

FIG. 24

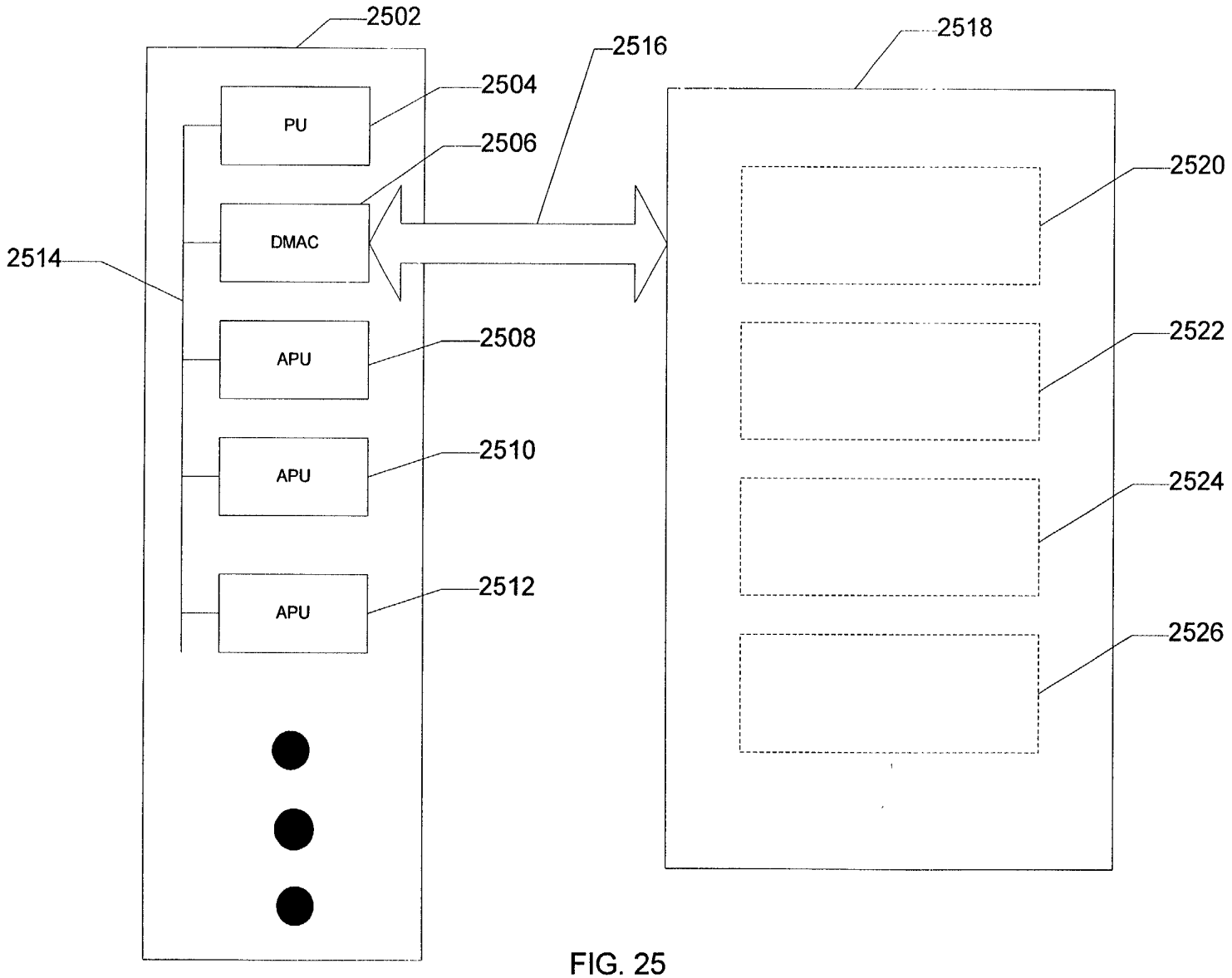

FIG. 25

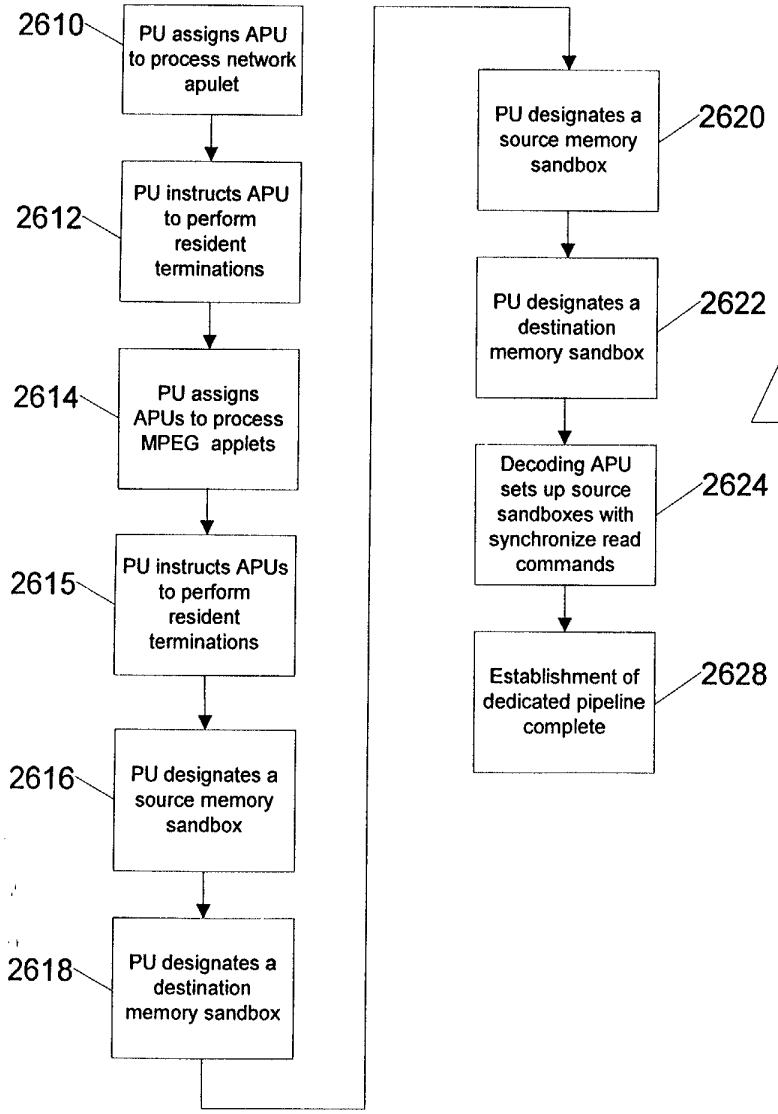

FIG. 26A

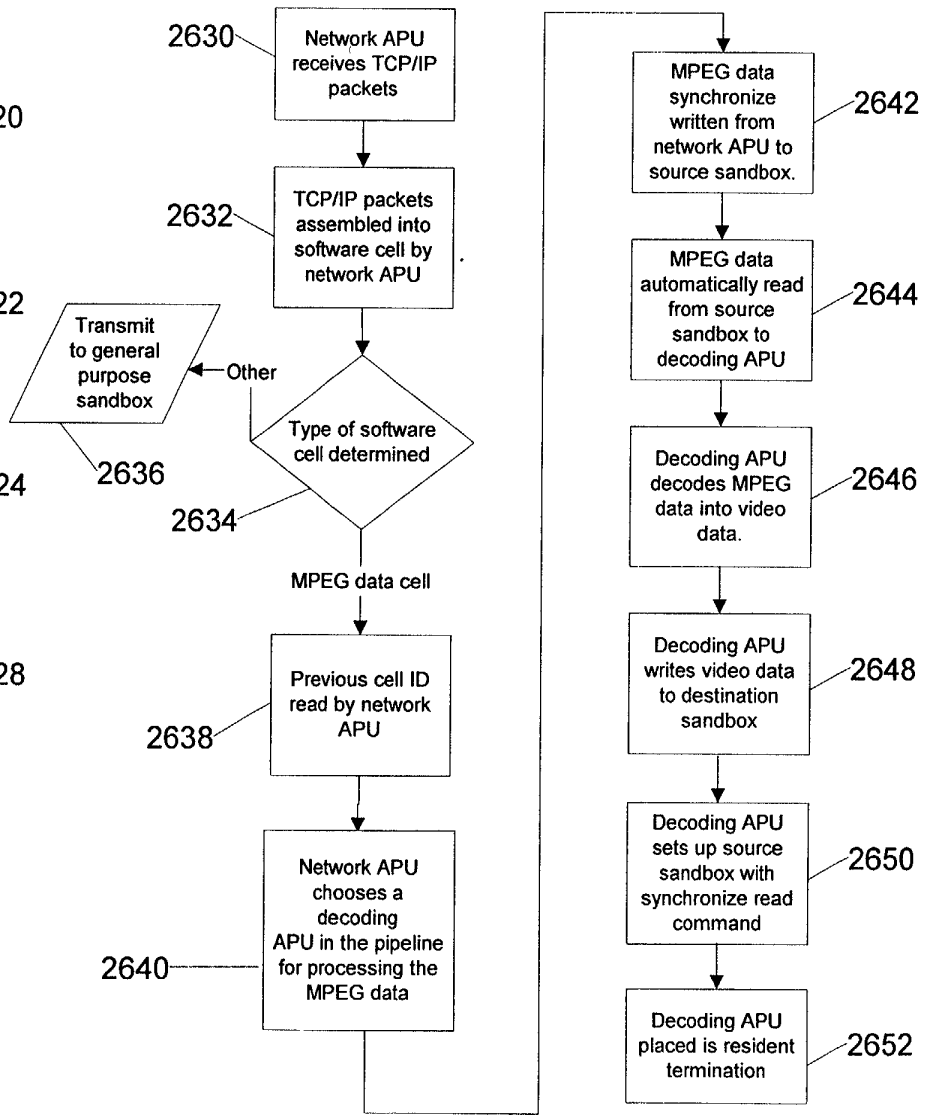

FIG. 26B

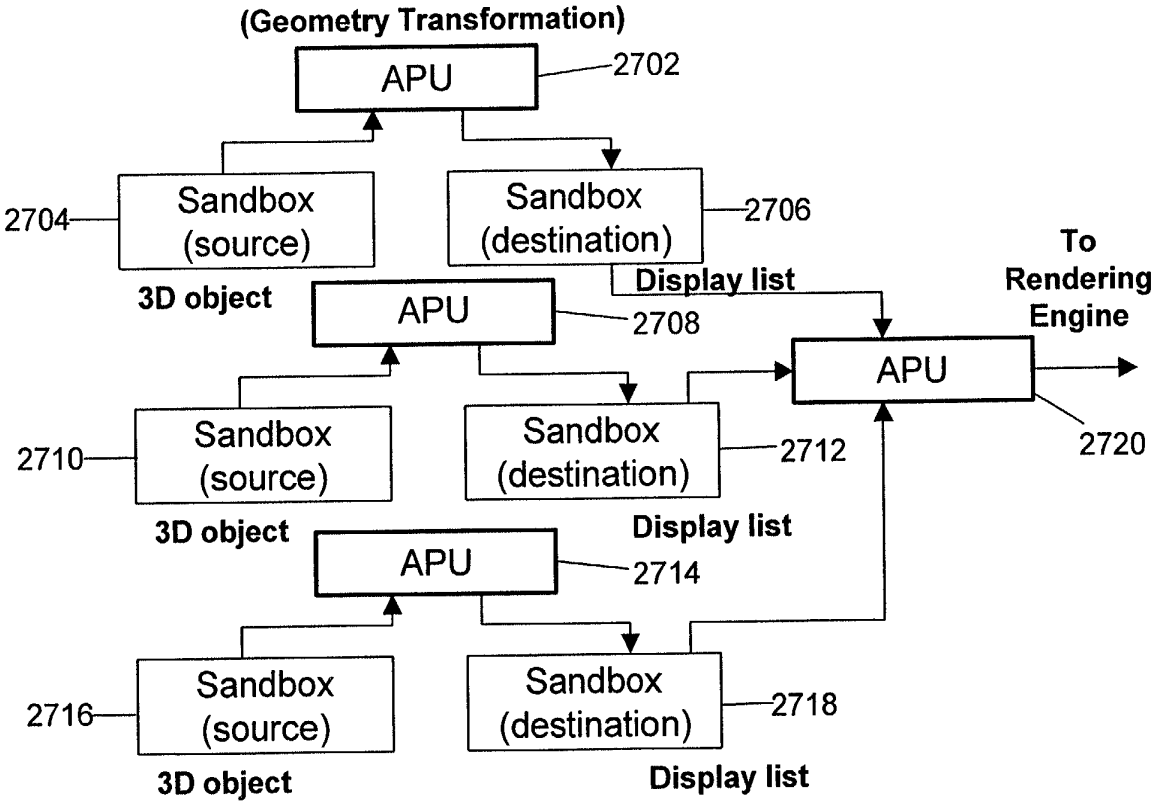

FIG. 27

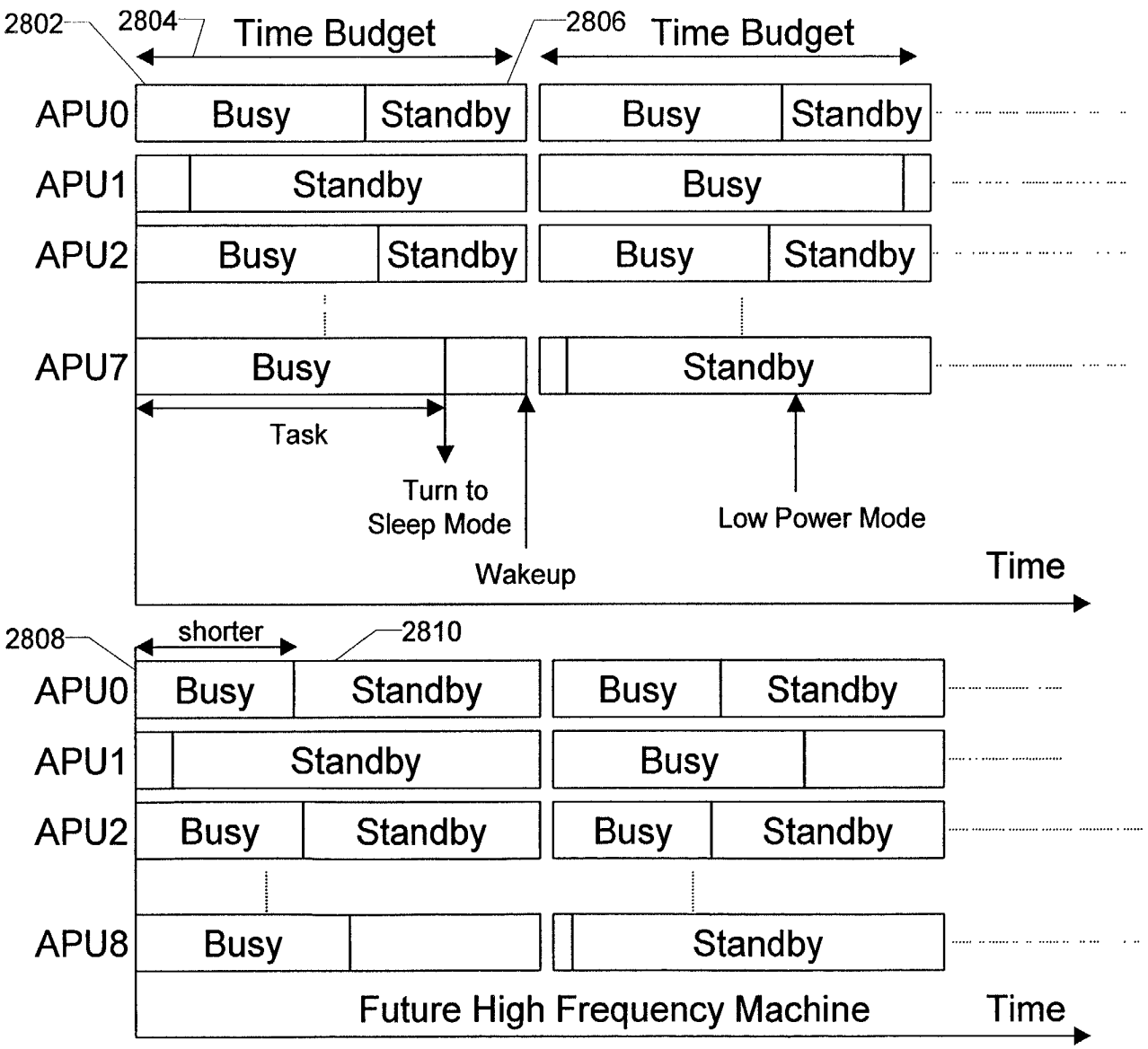
2802
2804
Time Budget
2806
Time Budget
APU0
Busy
Standby
Busy
Standby
APU1
Standby
Busy
APU2
Busy
Standby
Busy
Standby
APU7
Busy
Standby
Task
Turn to
Sleep Mode
Low Power Mode
Wakeup
Time
2808
shorter
2810
APU0
Busy
Standby
Busy
Standby
APU1
Standby
Busy
APU2
Busy
Standby
Busy
Standby
APU8
Busy
Standby
Future High Frequency Machine
Time

FIG. 28